

**File Name : LA-C371P**

# A4WAL M/B Schematics Document

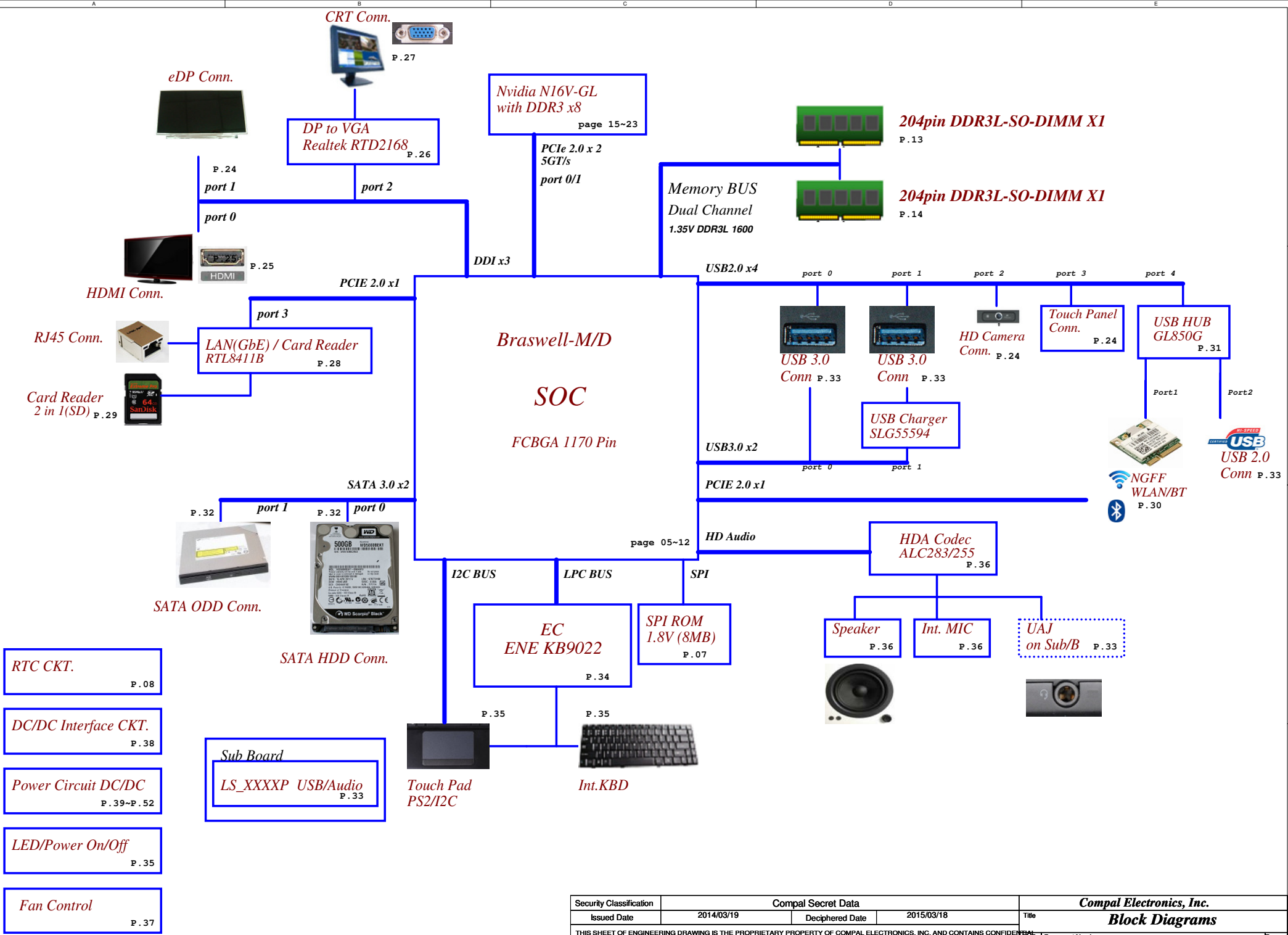
## Intel Braswell-M/D + N16X

2015-03-04

**REV:1.0**

Part Number	Description
DA6001BJ000	PCB 1BW LA-C371P REV0 MB 1

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/03/19	Deciphered Date	2015/03/18	Title	
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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
+19VB	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VALW	+1.05v Always power rail	ON	ON	ON
+1.15VALW	+1.15v Always power rail	ON	ON	ON
+1.24VALW	+1.24v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+3V_PTP	+3.3V power rail for PTP	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VGG	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
+3VSDGPU	+3.3V dGPU power rail	ON**	OFF	OFF
+VGA_CORE	Core voltage for dGPU	ON**	OFF	OFF
+1.5VSDGPU	+1.5V dGPU power rail	ON**	OFF	OFF
+1.05VSDGPU	+1.05V dGPU power rail	ON**	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				
Note : ON** dGPU optimus on				

Board ID / SKU ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

BOARD ID Table\_LA-C371P

Board ID	PCB Revision
01	EVT_LA-C371PR01
02	DVT_LA-C371PR02
03	PVT_LA-C371PR10

43 level BOM table

43 Level	Description	BOM Structure
4319X5BOL01	SMT MB AC371 A4WAL UMA HDMI	1DMIC@/255@/EMC@/HDD@/HUB@/NBYOC@/KB@/PCB@/LPC3V@/TSI@/UMA@/QHAX@
4319X5BOL02	SMT MB AC371 A4WAL DIS N16V-GM HDMI	1DMIC@/255@/EMC@/NGC6@/HDD@/HUB@/NBYOC@/KB@/PCB@/VGM@/LPC3V@/TSI@/VGA@/QHAW@
4319X5BOL03	SMT MB AC371 A4WAL DIS N16S-GT HDMI	1DMIC@/255@/EMC@/GC6@/HDD@/HUB@/NBYOC@/KB@/PCB@/SGT@/LPC3V@/TSI@/VGA@/QHAW@
4319X5BOL04	SMT MB AC371 A4WAL DIS N16V-GM 4G HDMI	1DMIC@/255@/EMC@/NGC6@/HDD@/HUB@/NBYOC@/KB@/PCB@/VGM@/LPC3V@/TSI@/VGA@/DR@/QHAW@
4319X5BOL05	SMT MB AC371 A4WAL DIS N16S-GT 4G HDMI	1DMIC@/255@/EMC@/GC6@/HDD@/HUB@/NBYOC@/KB@/PCB@/SGT@/LPC3V@/TSI@/VGA@/DR@/QHAW@
4319X5BOL06	SMT MB AC371 A4WAL UMA QHAW HDMI	1DMIC@/255@/EMC@/HDD@/HUB@/NBYOC@/KB@/PCB@/LPC3V@/TSI@/UMA@/QHAW@
4319X5BOL07	SMT MB AC371 A4WAL DIS GM2G QHAX HDMI	1DMIC@/255@/EMC@/NGC6@/HDD@/HUB@/NBYOC@/KB@/PCB@/VGM@/LPC3V@/TSI@/VGA@/QHAX@
4319X5BOL08	SMT MB AC371 A4WAL DIS GM4G QHAX HDMI	1DMIC@/255@/EMC@/NGC6@/HDD@/HUB@/NBYOC@/KB@/PCB@/VGM@/LPC3V@/TSI@/VGA@/DR@/QHAX@

EC SMBUS Routing Table

EC	Power	BAT	CHGR	SOC	DGPU
EC_SMB_CK1 EC_SMB_DA1	+3VALW	V	V	X	X
EC_SMB_CK2 EC_SMB_DA2	+3VS	X	X	V	V

SOC SMBUS Routing Table

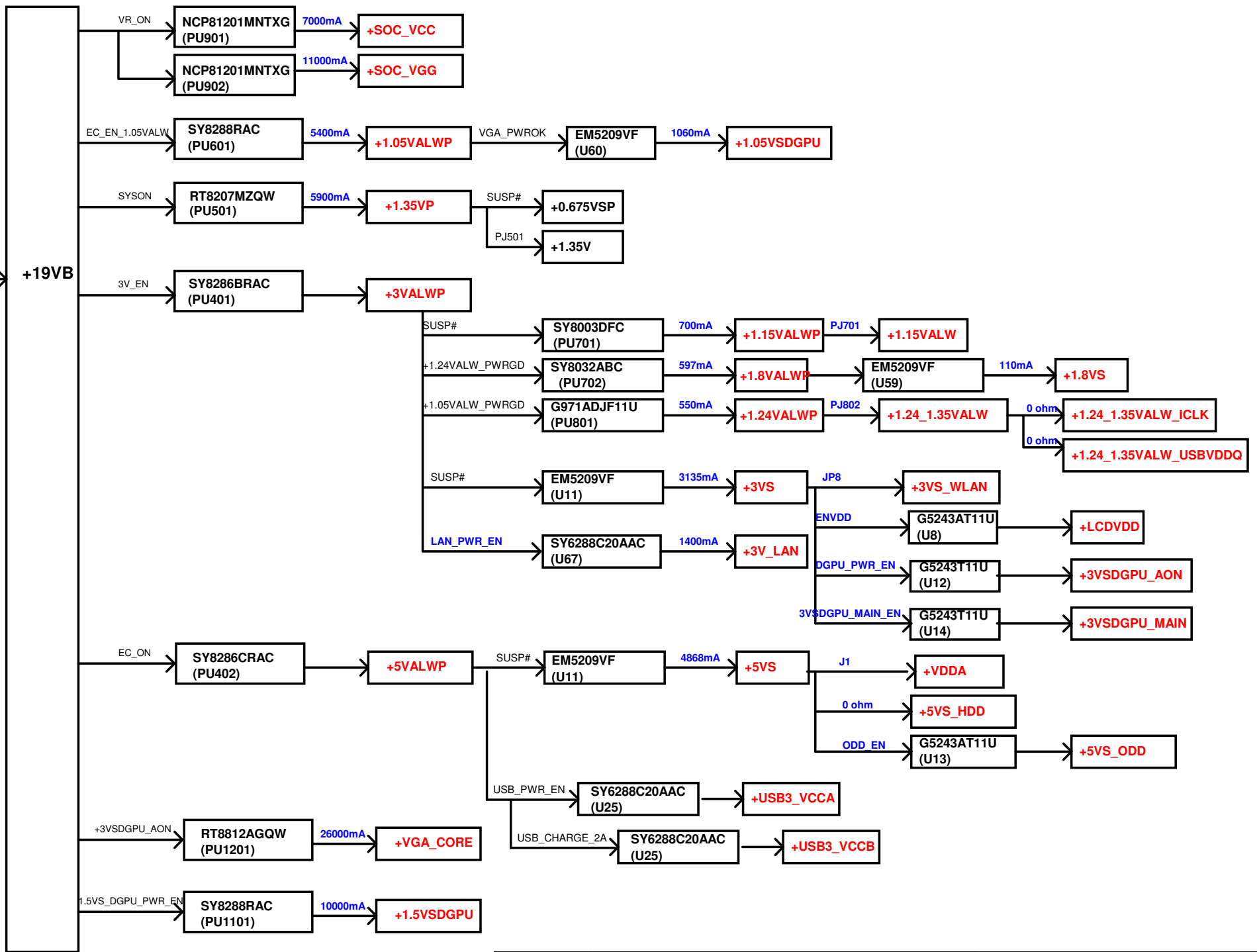
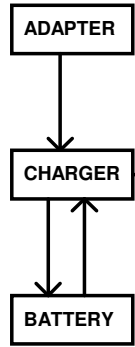
SOC	Power	DIMM1	DIMM2	NGFF	XDP	EC	DGPU	RTD2168
SMB Address								
SOC_SMBCLK SOC_SMBDATA	+1.8VALW to +3VS	V	V	V	X	V	V	V

I2C Map

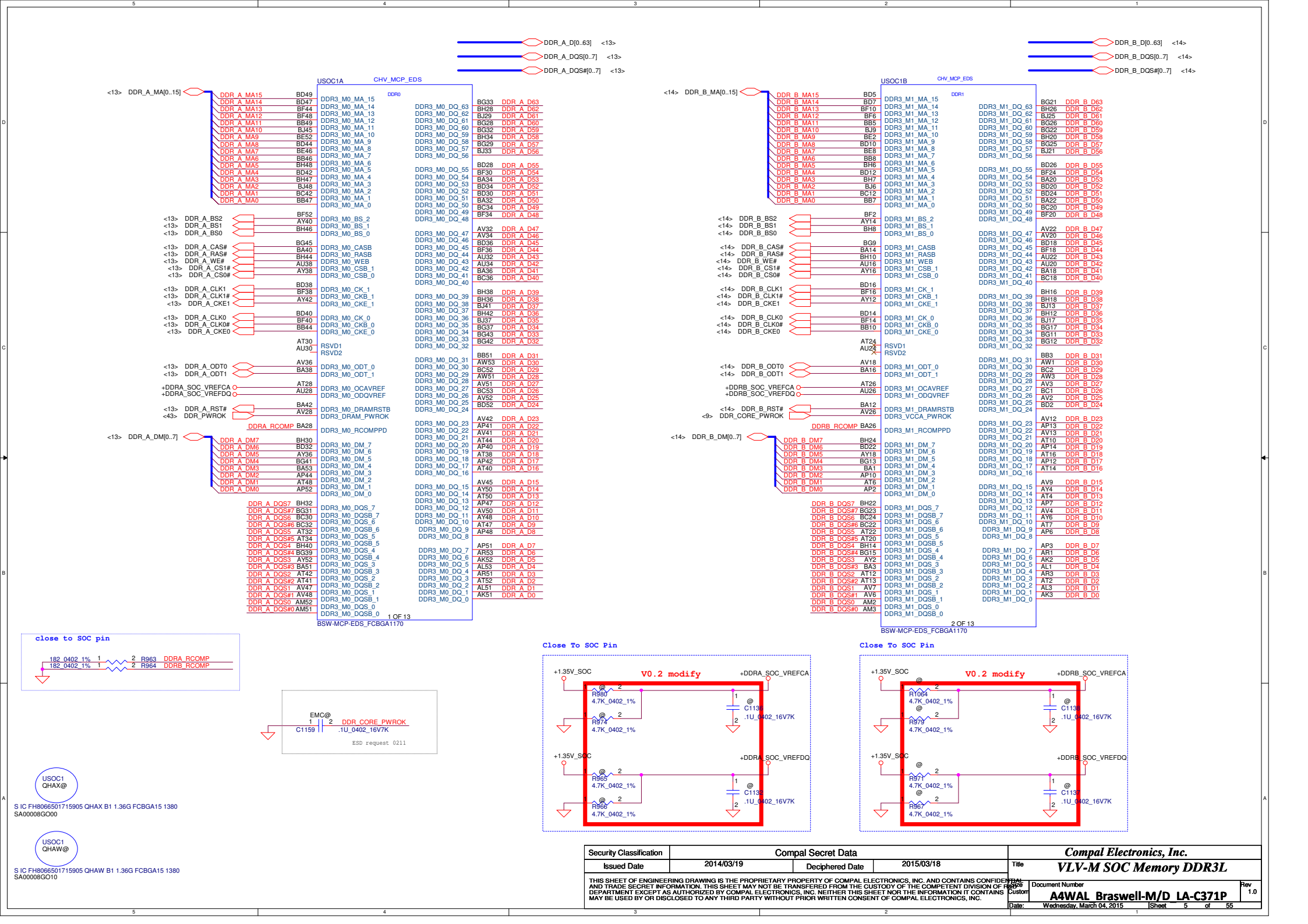
	Power	Touch PAD	Touch Panel
I2C Address		0xXX	0xXX
I2C Port2	+1.8VALW to +TS_PWR	X	V
I2C Port5	+1.8VALW to +3V_PTP	V	X

BOM Option Table		BOM Option Table	
Item	BOM Structure	Item	BOM Structure
Unpop	@	X76 VRAM	X76@
Connector	CONN@	with BYOC	BYOC@
EMC requirement	EMC@	without BYOC	NBYOC@
EMC requirement depop	@EMC@	EA Serial HDD	HDD@
Touch Screen I2C	TSI@	BA Serial HDD	BA@
KB BL	KB@	non USB HUB	NHUB@
TPM	TPM@	USB HUB	HUB@
NTPM	NTPM@	Dual Rank	DR@
Power Button	DBG@	G-sensor	GSEN@
dGPU	VGA@	CPU QHAX	QHAX@
N16S-GT SKU	SGT@	CPU QHAW	QHAW@
N16V-GM SKU	VGM@		
CODEC(ALC255)	255@		
CODEC(ALC283)	283@		
Non GPU CG6 Function	NGC6@		
GPU CG6 Function	GC6@		

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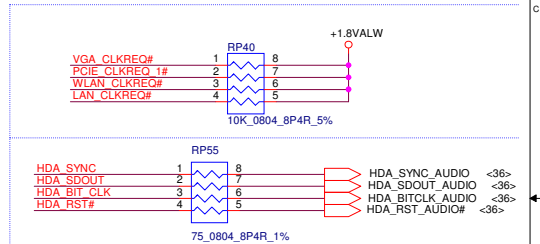


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Braswell	Acer 2015
USB3 Port1	USB 3 (I/O)
USB3 Port2	USB 3 (I/O)
PCIe Port0	dGPU/M.2 PCIE
PCIe Port1	LAN
PCIe Port2	WIFI
PCIe Port3	LAN+CR



+BIOS\_SPI

R999 1 2 3.3K 0402 5% SPI CS#

R1001 1 2 20K 0402 5% SPI WP#

R1000 1 2 20K 0402 5% SPI HOLD#

The schematic diagram shows the BIOS\_SPI signal path. The BIOS\_SPI pin is connected to the SPI pin of the R998 chip. The R998 chip is connected to the +1.8V\_ALW pin. A capacitor C1013 is connected between the SPI pin of R998 and ground.

Diagram illustrating the pin connections for the 10\_0804\_8P4R\_5% component:

- SOC SPI CS0# 1 EMC@ 2 SPI CS0# 33 0402\_5%
- SOCI WP# 2 EMC@ 2 SPI WP# 10\_0402\_5%
- SOCI HOLD# 4 5 SPI HOLD# 5
- SOCI MOSI 3 6 SPI MOSI 6
- SOCI MISO 7 7 SPI MISO 7
- SOCI CLK 1 8 SPI CLK 8
- 10\_0804\_8P4R\_5%
- EMC@

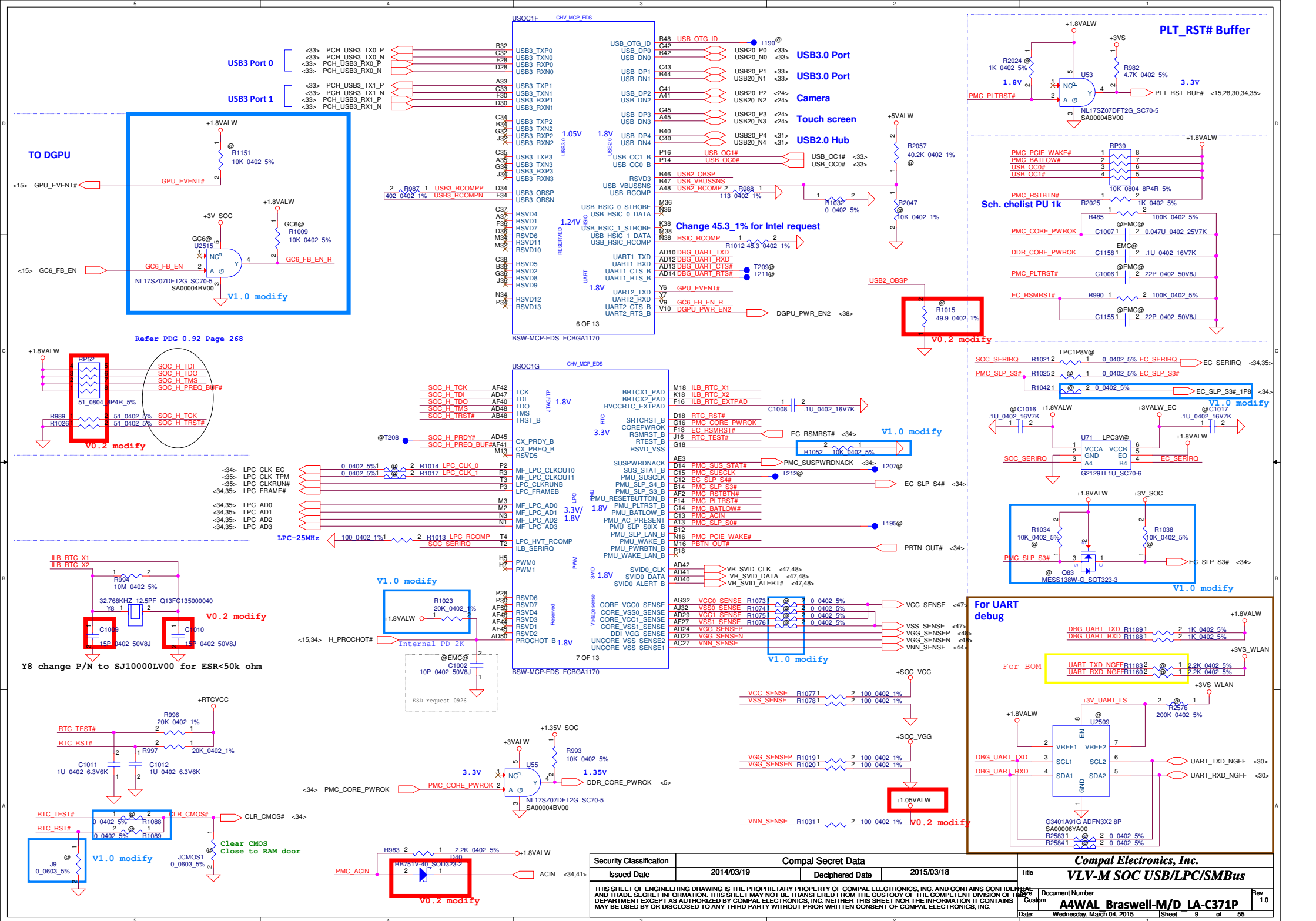
U56		+BIOS_SPI			
SPI_CS0#	1	CS#	VCC	8	SPI_HOLD#
SPI_MISO	2	DO(IQ1) HOLD#(IQ3)		7	SPI_CLK
SPI_WP#	3	WP#(IQ2)	CLK	6	SPI_MOSI
	4	GND	DI(IQ0)	5	

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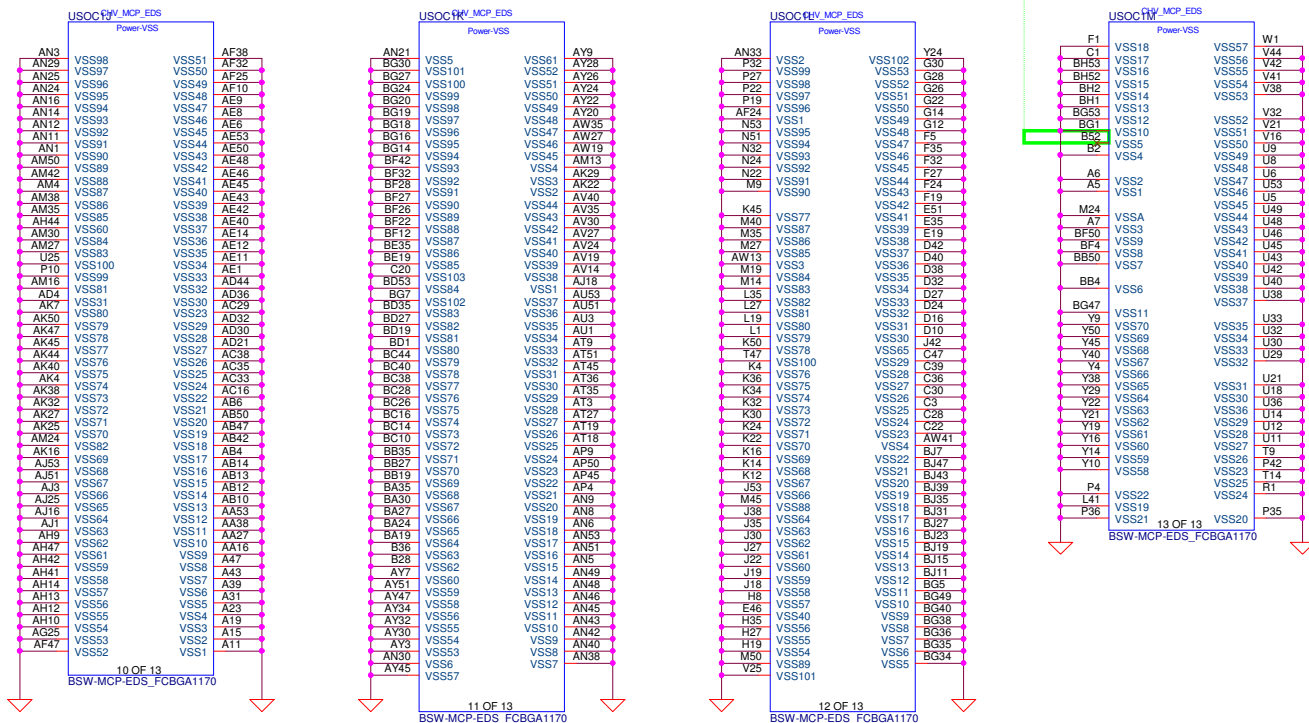












ball\_B52 :  
if connect to GND , layout side need use 3mil-core and will cost up ,  
so left NC pin\_B52 (Intel CRB also left NC)



All VREF traces should have 10 mil trace width

Swap D4->D5, D5->D6, D6->D4

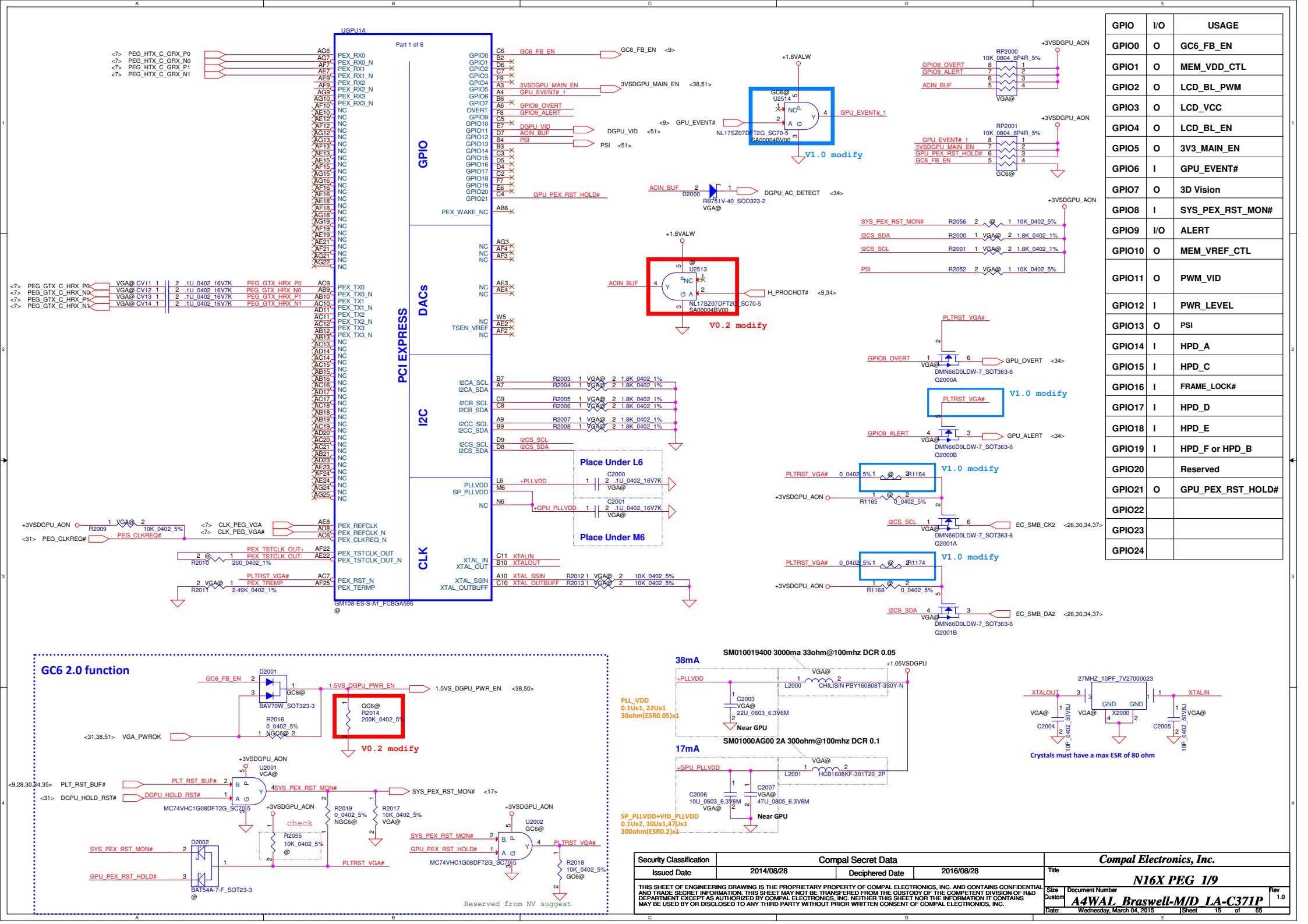
## Channel B

SA0/SA1 Follow INTEL demo board

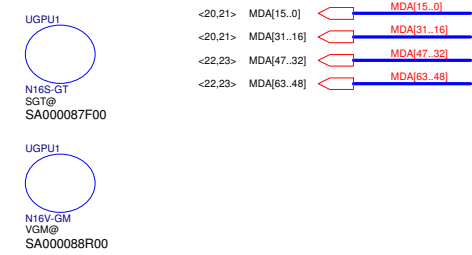
<Address: SA0:SA1=10 (A2H)>  
DIMM\_2 STD H:4mm

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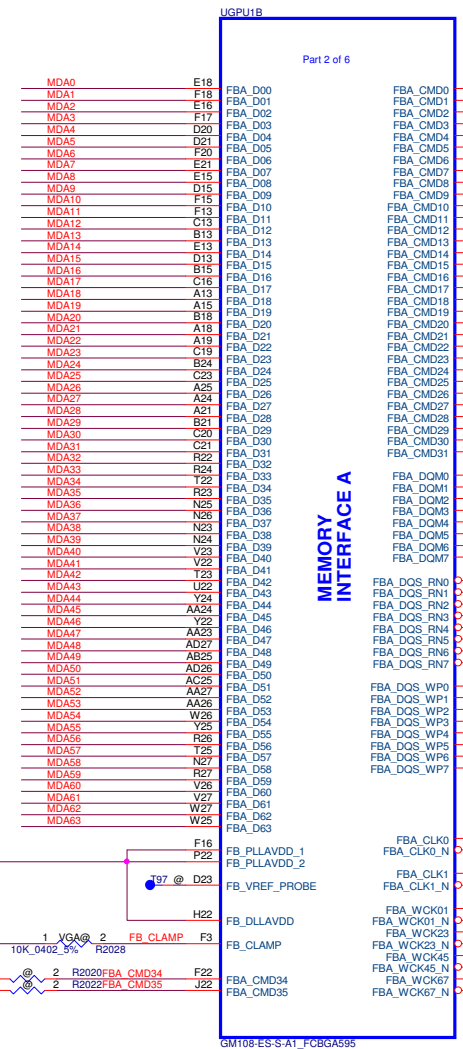
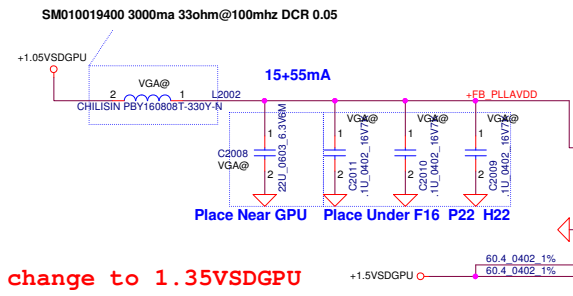


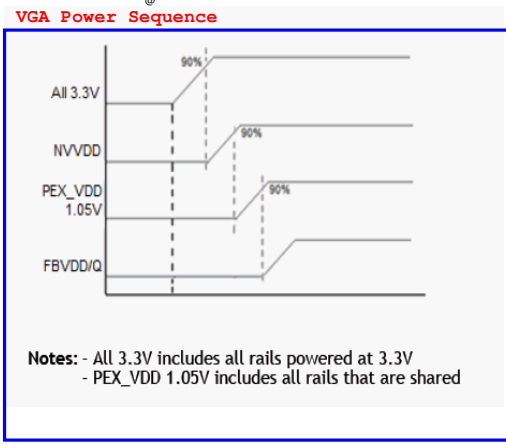
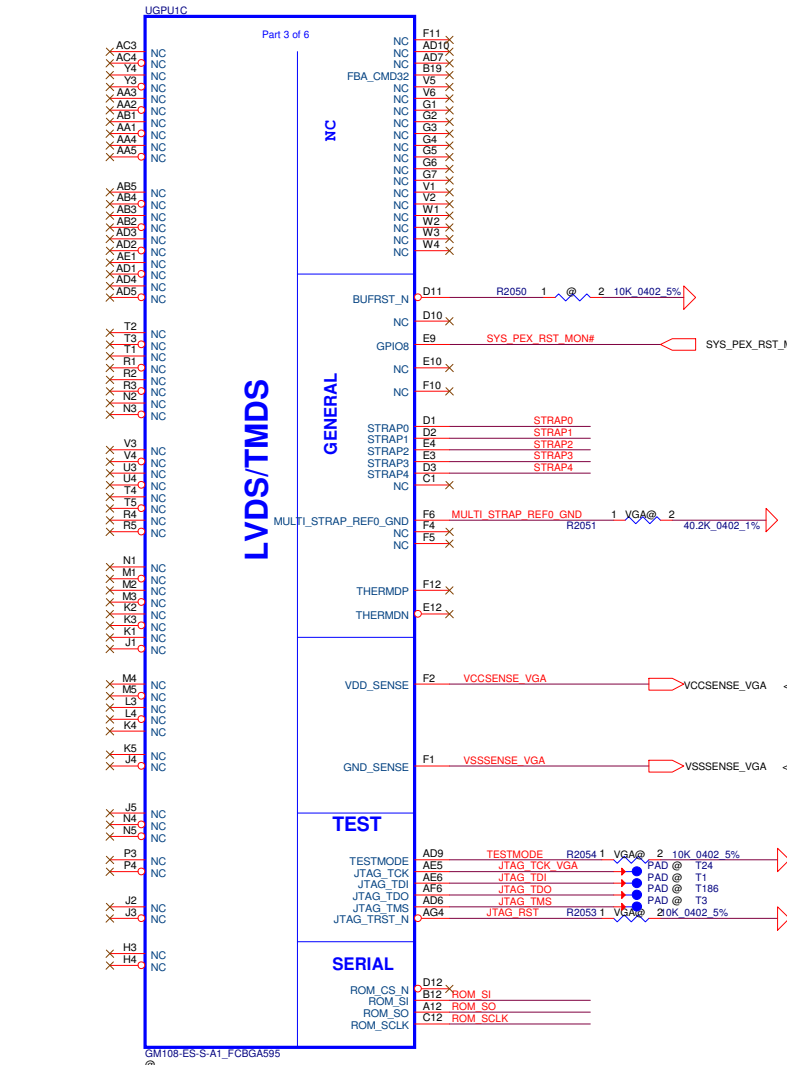
VRAM Interface



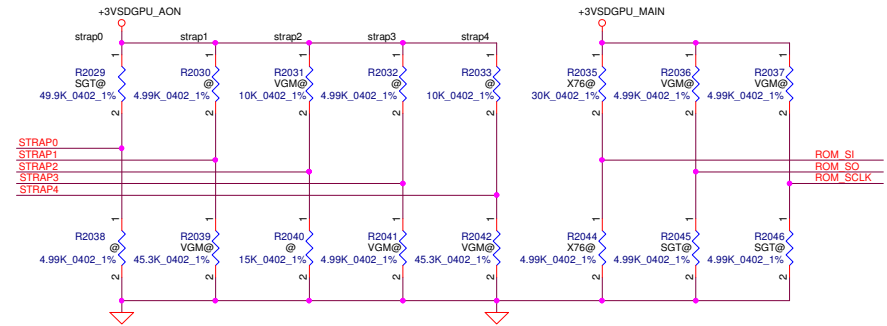
NV 15x DG-06803-V03  
NV 16x DG-07158-V04

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 μF	X7R	0402	2	Under GPU
		22 μF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU





## MULTI LEVEL STRAPS



N16VGM Option Component

STRAP0 ----> R2029 2 VGM@ 1 45.3K\_0402\_1% SD034453280

## For N16S-GT Binary strap table

Decive ID : 0x1347

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16S-GT	+1.5V	Dual	X76615BOL13	1GHz	256Mx16x8 4G	0xG (SA00008DN10) Hynix H5TC4G63CFR-NOC	PU 49.9K	NC	NC	NC	NC	PU 24.9K	PD 4.99K	PD 4.99K
			X76615BOL12			0x1 (SA000077K20) Micron MT41J256M16HA-093G.E						PD 10K		
			X76615BOL05			0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
	+1.5V	Single	X76615BOL03	1GHz	256Mx16x4 2G	0x5 (SA00008DN10) Hynix H5TC4G63CFR-NOC						PD 30.1K		
			X76615BOL11			0x1 (SA000077K20) Micron MT41J256M16HA-093G.E						PD 10K		
			X76615BOL04			0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		

## For N16V-GM Binary strap table

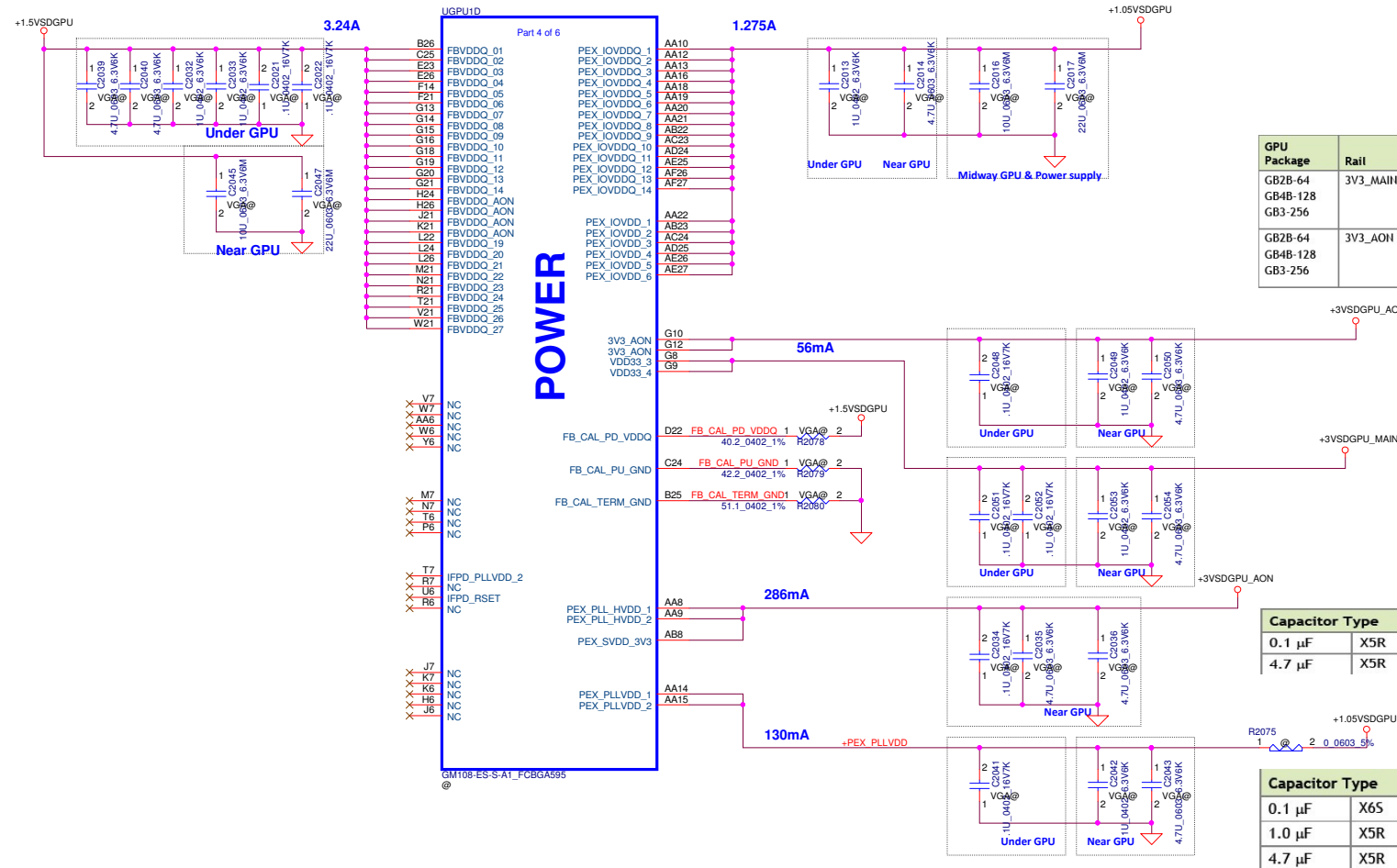
Decive ID : 0x1299

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16V-GM	+1.35V	Dual	X76615BOL09	900MHz	256Mx16x8 4G	0xA (SA00008DN10) Hynix H5TC4G63CFR-NOC	PU 45.3K	PD 45.3K	PU 10K	PD 4.99K	PD 45.3K	PU 15K	PU 4.99K	PU 4.99K
			X76615BOL08			0xD (SA000077K20) Micron MT41J256M16HA-093G.E						PU 30.1K		
			X76615BOL10			0xG (SA000076P20) Samsung K4W4G1646D-BC1A						PU 24.9K		
	+1.5V	Single	X76615BOL01	1GHz	256Mx16x4 2G	0x9 (SA00008DN10) Hynix H5TC4G63CFR-NOC						PU 10K		
			X76615BOL07			0x1 (SA000077K20) Micron MT41J256M16HA-093G.E						PD 10K		
			X76615BOL02			0x4 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 24.9K		

**NV 16x DG-07158-V04**

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64 DDR3	0.1 $\mu$ F	X7R	0402	2	2	Under GPU
	1 $\mu$ F	X7R	0603	2	2	Under GPU
	4.7 $\mu$ F	X6S	0603	2	2	Under GPU
	10 $\mu$ F	X5R	0805	1	1	Near GPU
	22 $\mu$ F	X5R	0805	1	1	Near GPU

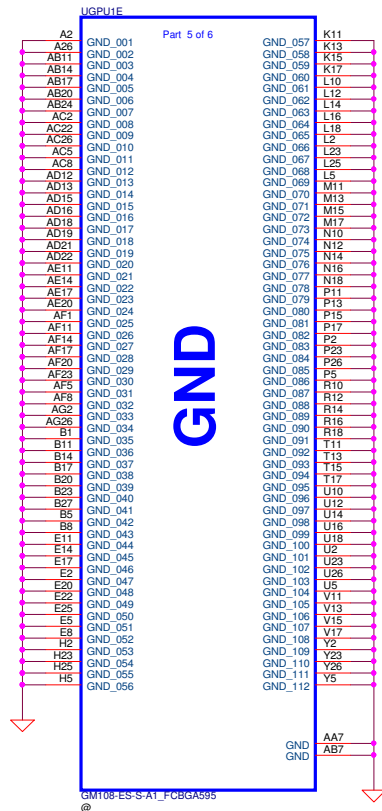
GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64	1.0 $\mu$ F X6S	0402	1	Under GPU
	4.7 $\mu$ F X6S	0603	1	Near GPU
	10 $\mu$ F X5R	0805	1	Midway between GPU and Power Supply
	22 $\mu$ F X5R	0805	1	Midway between GPU and Power Supply



GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AOH	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 $\mu$ F	X5R	0402	1	Near GPU
4.7 $\mu$ F	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 $\mu$ F	X6S	0402	1	Under GPU
1.0 $\mu$ F	X5R	0603	1	Near GPU
4.7 $\mu$ F	X5R	0805	1	Near GPU



## NV 15x DG-06803-V03

## NV 16x DG-07158-V04

GPU Package Type	Capacitor Type	Footprint	Population	Location	Comments
GB2B-64	4.7 $\mu$ F	X6S	0603	10	10
	1 $\mu$ F	X6S	0402	4	4
	47 $\mu$ F	X5R	0805	1	1
	22 $\mu$ F	X5R	0805	1	1
	4.7 $\mu$ F	X5R	0805	5	5
	330 $\mu$ F	POS	7343	1	1
					ESR $\leq$ 6 m $\Omega$

## DA-07312-V02

Table 6. EDP-Peak <sup>3</sup>

Products	VRM Type	GPU Core		GPU FBIO		FB Total <sup>1,5</sup>	1.05V Total <sup>2</sup>
		—	1.5V <sup>4</sup>	1.35V <sup>4</sup>	1.5V <sup>4</sup>	1.35V <sup>4</sup>	1.05V <sup>4</sup>
H165-GT	DDR3/L	51	2.56	2.18	4.08	3.63	2.09
H165-GM	DDR3/L	32	2.56	2.18	4.08	3.62	2.09
H165-LP	DDR3L	29	N/A	2.13	N/A	3.54	2.09

### Notes:

1. FB Total = GPU FBIO + VRAM IO + VRAM Core = FBVDD + FBVDDQ
2. 1.05V Total includes the PCIe and other 1.05V power rails.
3. Worst case current is observed at the temperature of the GPS Thermal Control Limit defined in Table 3.
4. Power supply rail voltages set to maximum DC tolerance.
5. VRAM Total power is for reference only. For absolute ratings, please contact VRAM manufacturer.

## DA-07314-V02

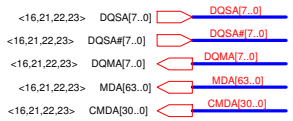
Table 6. EDP-Peak <sup>3</sup>

Products	VRM Type	GPU Core		FB Total <sup>1,5</sup>	1.05V Total <sup>2</sup>
		—	1.5/1.35V <sup>4</sup>	1.5/1.35V <sup>4</sup>	1.05V <sup>4</sup>
H16V-GM	DDR3/L	40.97	3.87	5.86	1.74

### Notes:

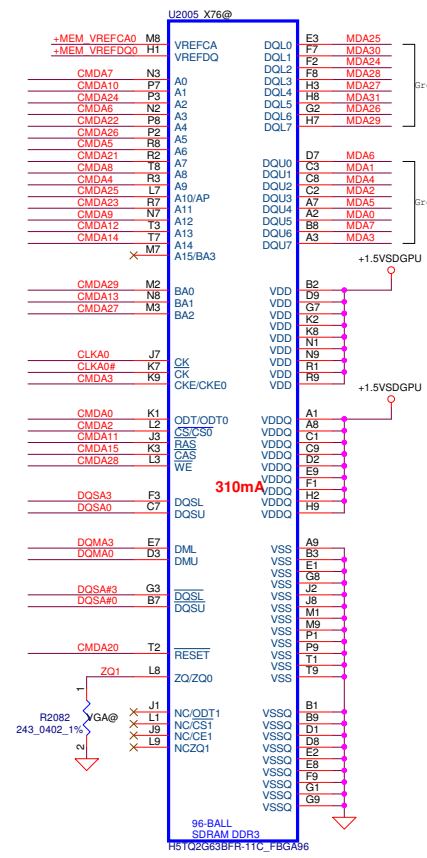
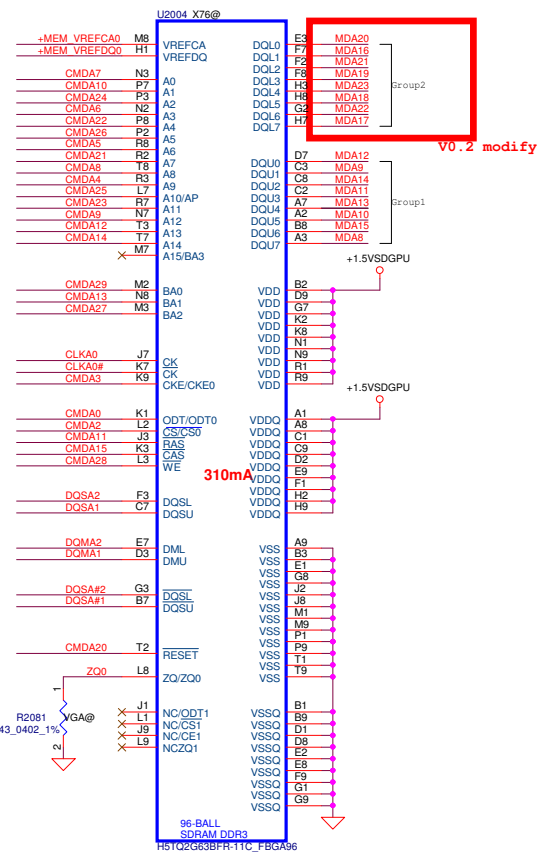
1. FB Total = GPU FBIO + VRAM IO + VRAM Core = FBVDD + FBVDDQ
2. 1.05V Total includes the PCIe and other 1.05V power rails.
3. Worst case current is observed at the temperature of the GPS Thermal Control Limit defined in Table 3.
4. Power supply rail voltages set to maximum DC tolerance.
5. VRAM Total power is for reference only. For absolute ratings, please contact VRAM manufacturer.

VRAM DDR3 chips



Lower Rank 0 BOT SIDE

X76

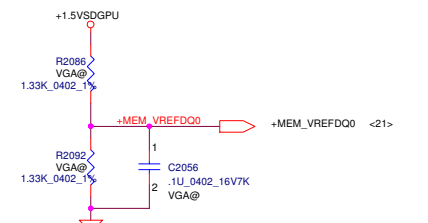
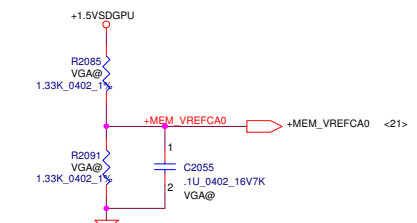
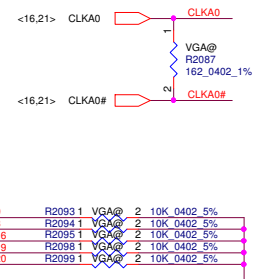
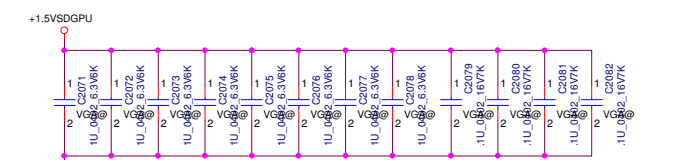


Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17			CS1*	
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

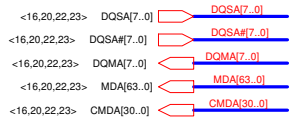
Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type		Population		Location
		FBVDDQ	FBVDD	
FBVDD/Q Combined				
0.1 µF	X7R	0402	2	Under DRAM
1.0 µF	X7R	0603	4	Under DRAM
10 µF	X5R	0805	0	Close to DRAM

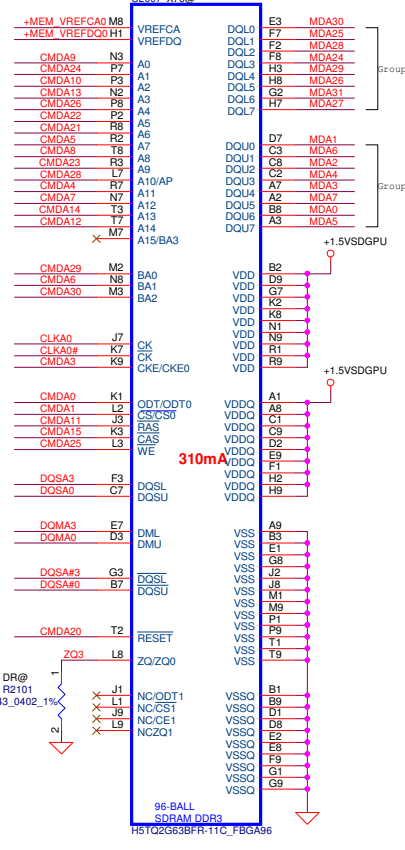
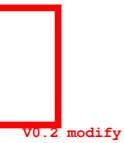
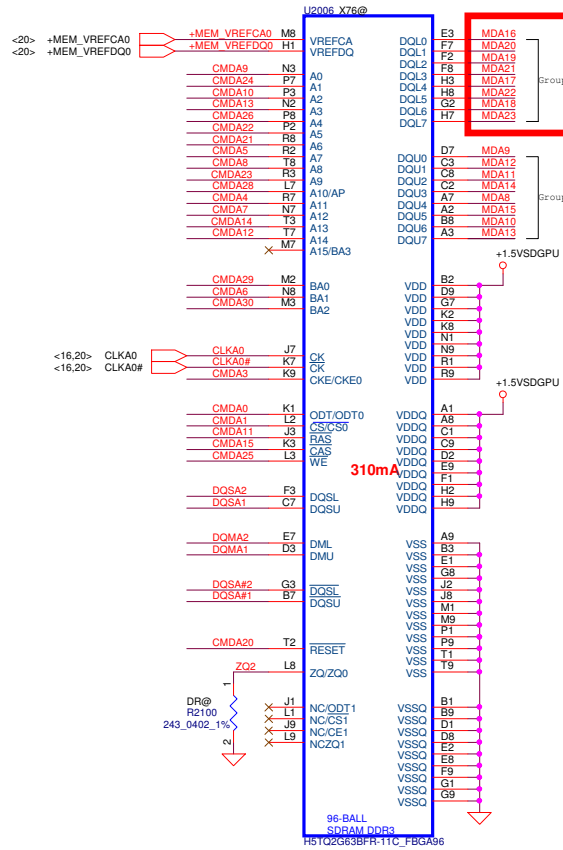




# VRAM DDR3 chips

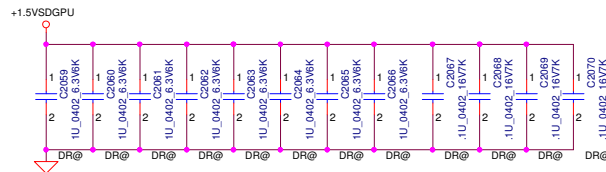


## Lower Rank 1 TOP SIDE



Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

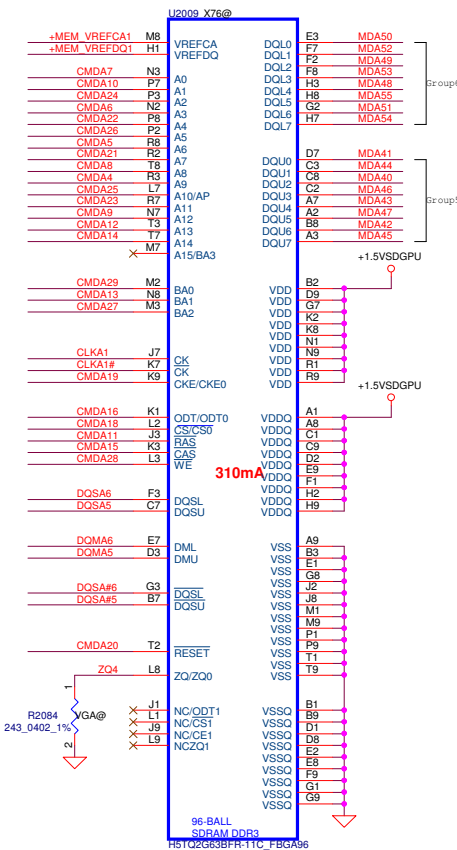
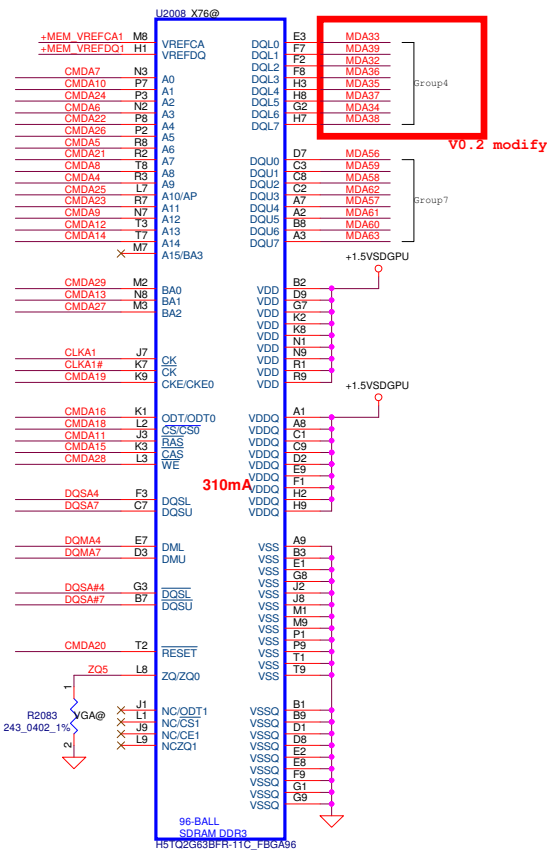


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				Document Number	A4WAL Braswell-M/D LA-C371P
				Date	Wednesday, March 04, 2015
				Sheet	21 of 55
				Rev	1.0

# VRAM DDR3 chips

<16,20,21,23> DQSA[7..0] DQSA[7..0]  
 <16,20,21,23> DQSA[7..0] DQSA[7..0]  
 <16,20,21,23> DQMA[7..0] DQMA[7..0]  
 <16,20,21,23> MDA[63..0] MDA[63..0]  
 <16,20,21,23> CMDA[30..0] CMDA[30..0]

## Upper Rank 0 BOT SIDE



Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17			CS1*	
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

DDR3	Command Bit	Default Pull-down
	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

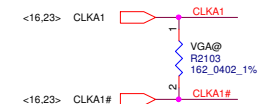
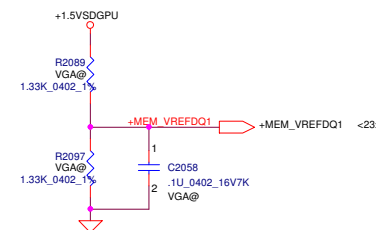
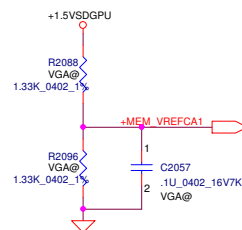
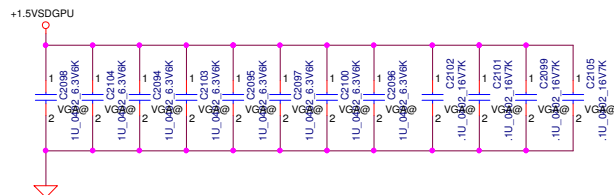
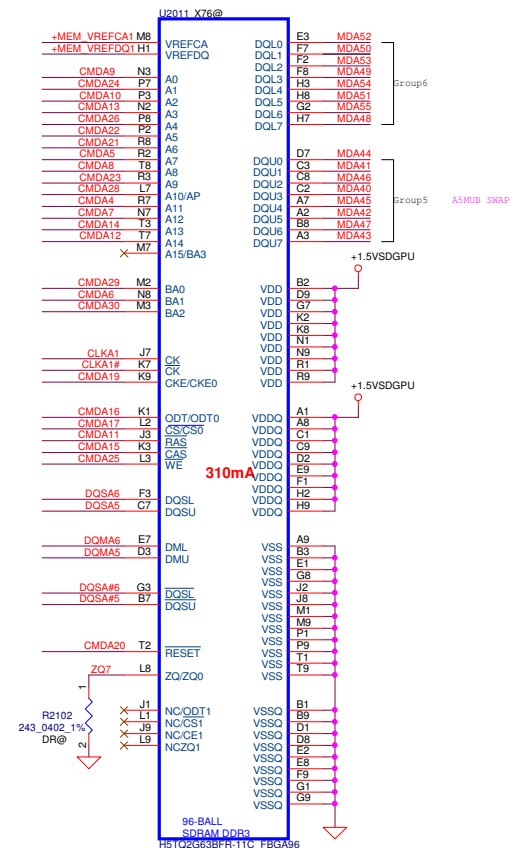
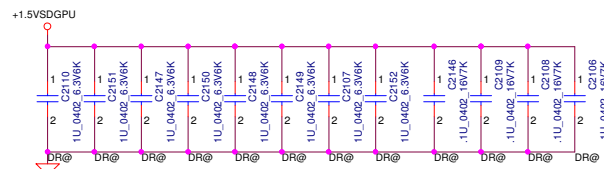


Figure 1 illustrates the comparison of the proposed DQSA and DQMA with the existing MDA and CMDA. The diagram shows four rows of communication links between a source (left) and a destination (right). Each row represents a different scheme: DQSA, DQMA, MDA, and CMDA. The source and destination are represented by blue rectangles. The links are represented by red arrows. The DQSA and DQMA schemes show a single link from the source to the destination, while the MDA and CMDA schemes show multiple links (indicated by multiple arrows) from the source to the destination.

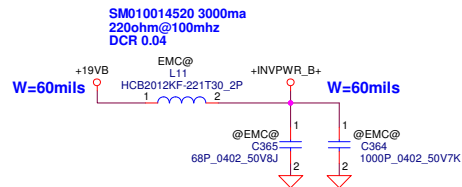
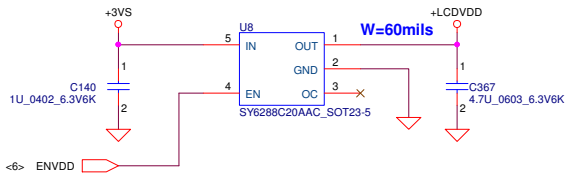


Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

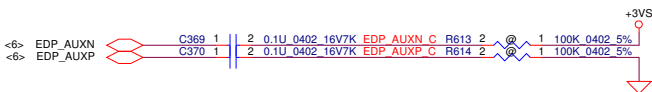
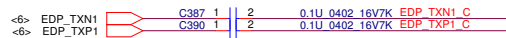
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



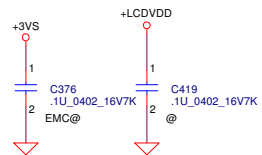
## LCD POWER CIRCUIT



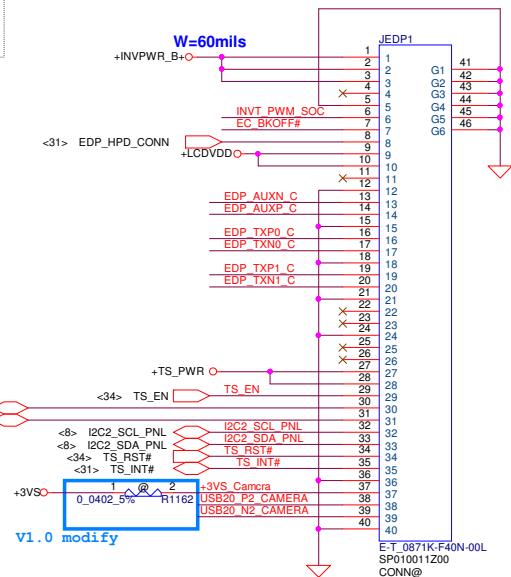
eDP



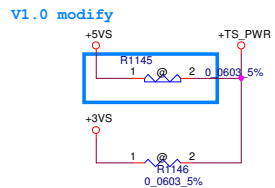
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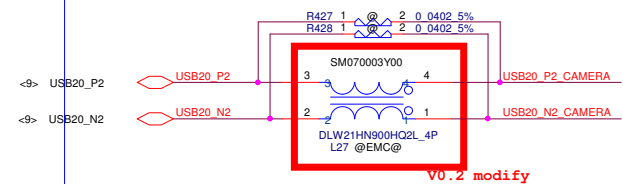
**LCD/ LED PANEL Conn.**



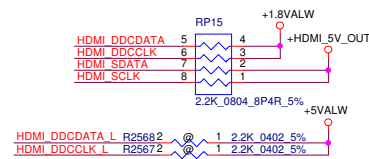
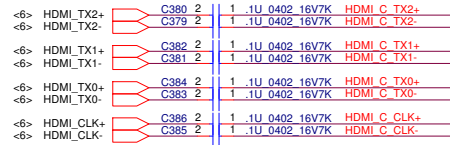
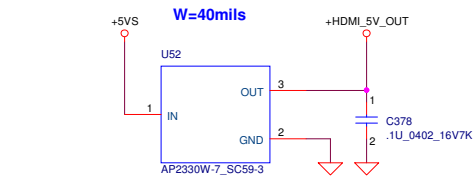
### For Touch Panel



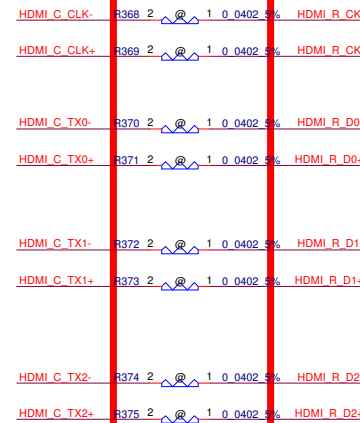
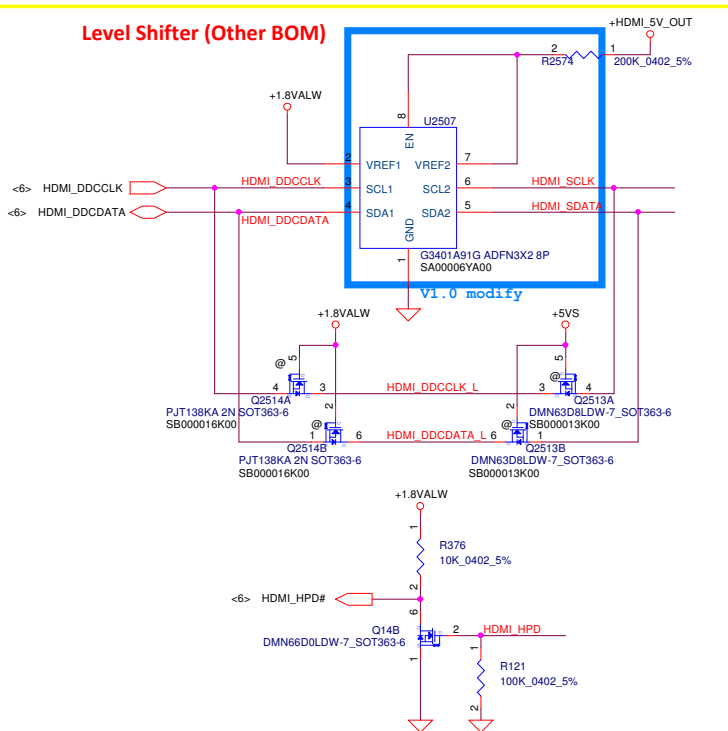
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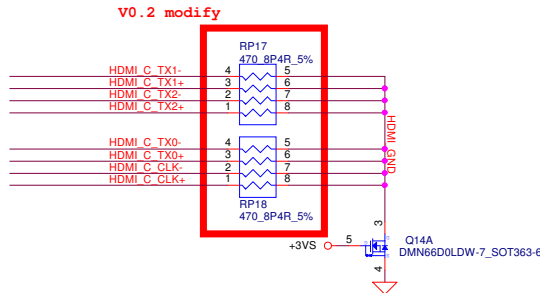
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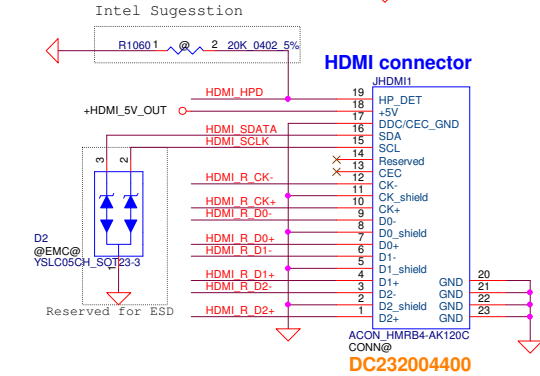
### Level Shifter (Other BOM)



V0.2 modify



V0.2 modify



ZZZ1  
HDMI ROYALTY  
ROYALTY HDMI W/LOGO+HDCP  
RO0000003HM  
45@

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				Document Number				A4WAL Braswell-M/D LA-C371P			
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# CRT conn.

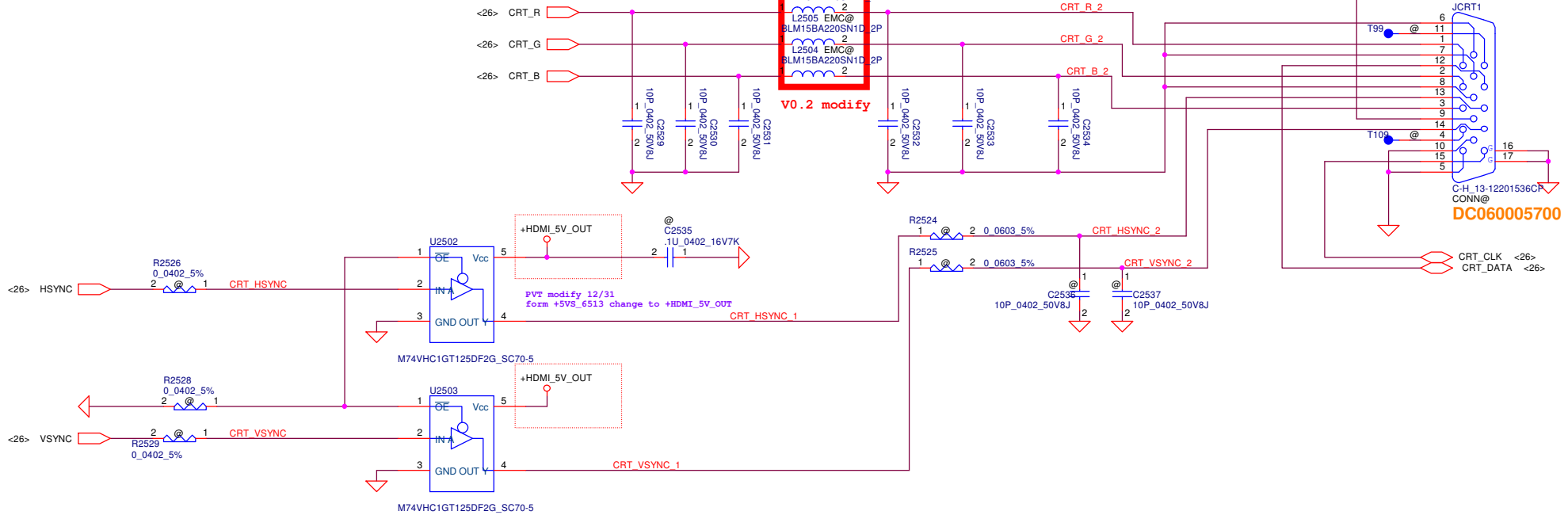
SM01000LU00 ( S SUPPRE\_ MURATA BLM15BA220SN1D 0402)

L2503 EMC@  
BLM15BA220SN1D 2P  
L2505 EMC@  
BLM15BA220SN1D 2P  
L2504 EMC@  
BLM15BA220SN1D 2P

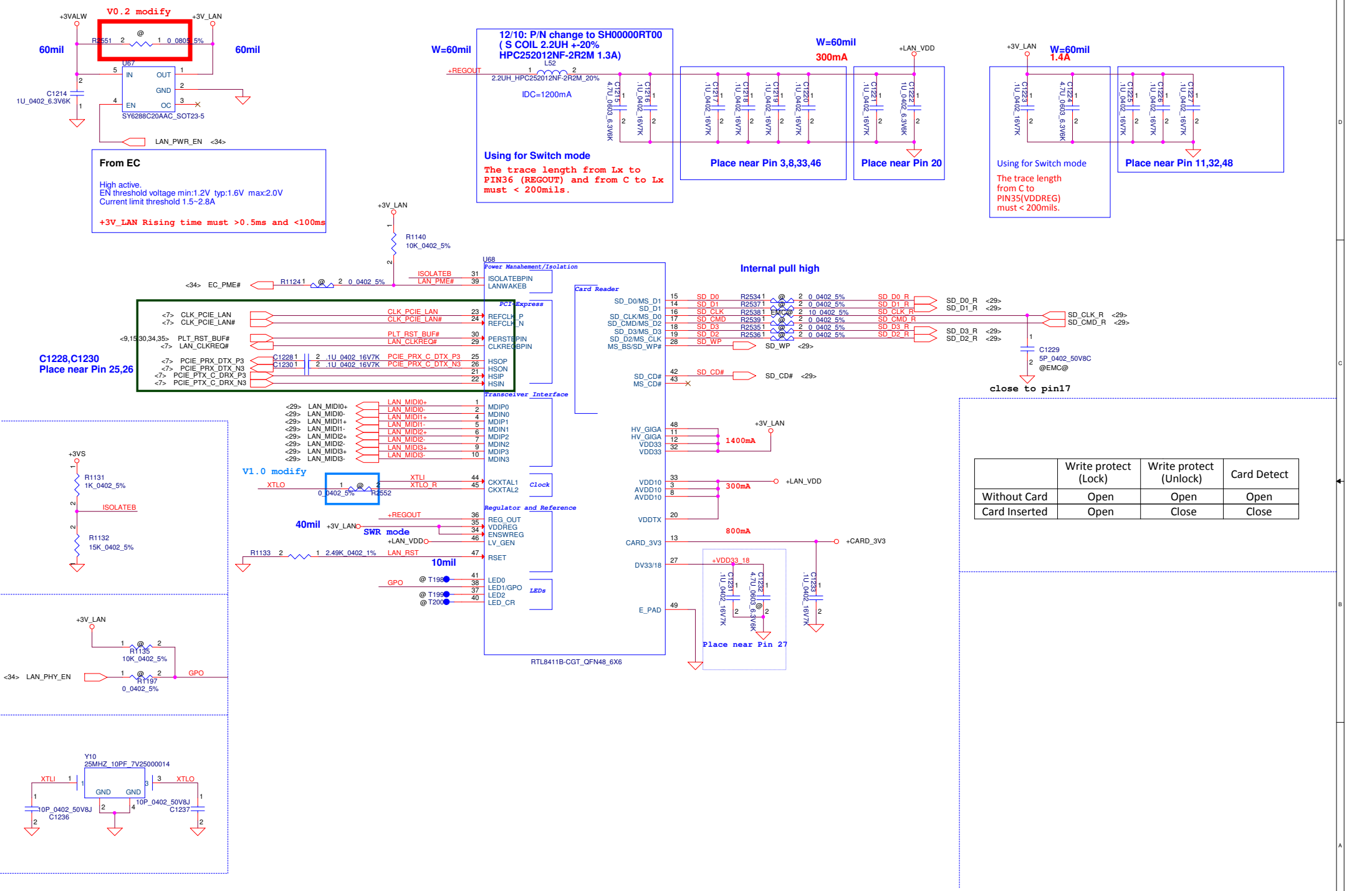
V0.2 modify

W=40mils  
+HDMI\_5V\_OUT

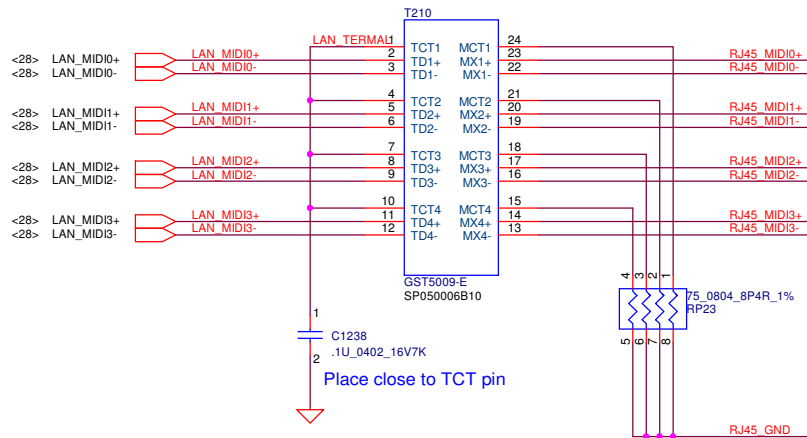
CRT Connector



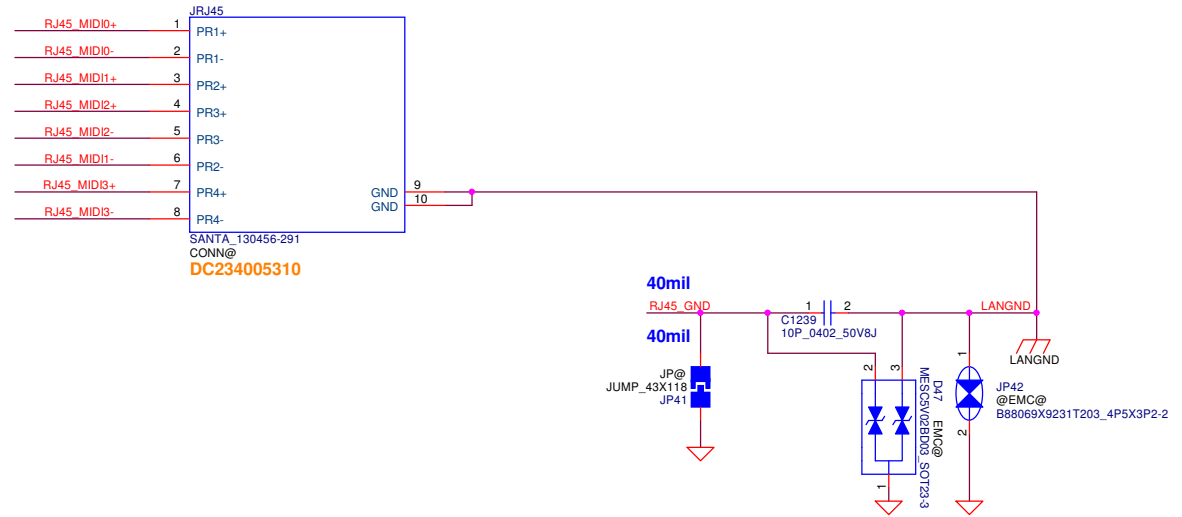
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					Size	
					Document Number	
					Rev	
					1.0	
					A4WAL Braswell-M/D LA-C371P	
Date:		Wednesday, March 04, 2015		Sheet	27	of 55



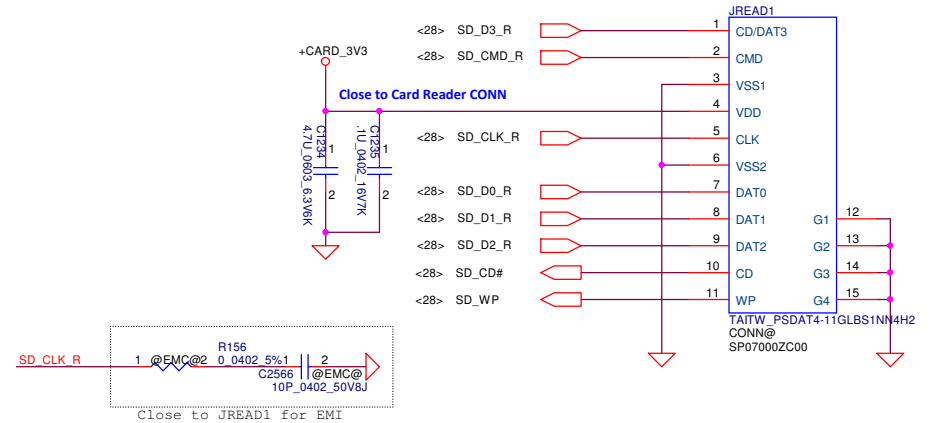
	Write protect (Lock)	Write protect (Unlock)	Card Detect
Without Card	Open	Open	Open
Card Inserted	Open	Close	Close



## LAN Connector



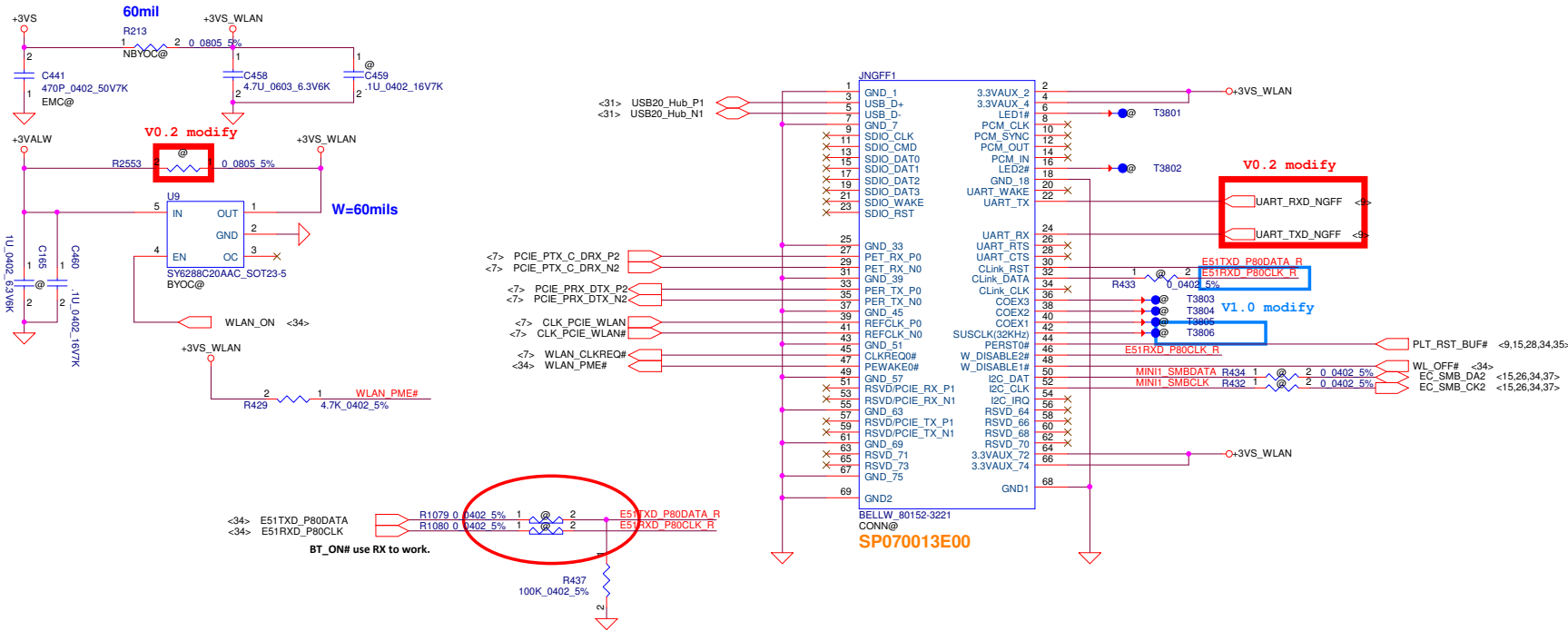
## Card Reader Connector



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Size Custom	Document Number	A4WAL Braswell-M/D LA-C371P		Rev 1.0
Date:	Wednesday, March 04, 2015	Sheet	29	of 55

# For Wireless LAN

## NGFF WL+BT (KEY E)

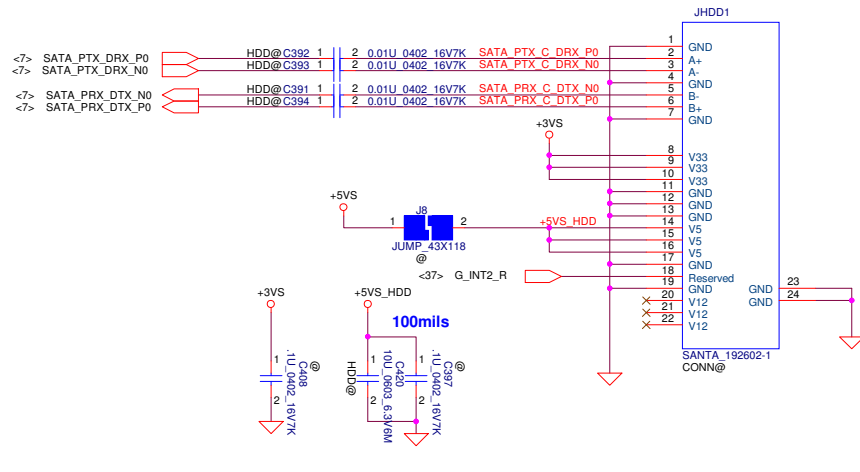


74	1.0	UND	75
72	1.0	RESERVED/REFCLK	73
70	1.0	RESERVED/REFCLK	71
68	1.0	RESERVED/REFCLK	69
66	1.0	RESERVED/REFCLK	67
64	1.0	RESERVED/REFCLK	65
62	1.0	RESERVED/REFCLK	63
60	1.0	RESERVED/REFCLK	61
58	1.0	RESERVED/REFCLK	59
56	1.0	RESERVED/REFCLK	57
54	1.0	RESERVED/REFCLK	55
52	1.0	RESERVED/REFCLK	53
50	1.0	RESERVED/REFCLK	51
48	1.0	RESERVED/REFCLK	49
46	1.0	RESERVED/REFCLK	47
44	1.0	RESERVED/REFCLK	45
42	1.0	RESERVED/REFCLK	43
40	1.0	RESERVED/REFCLK	41
38	1.0	RESERVED/REFCLK	39
36	1.0	RESERVED/REFCLK	37
34	1.0	RESERVED/REFCLK	35
32	1.0	RESERVED/REFCLK	33
30	1.0	RESERVED/REFCLK	31
28	1.0	RESERVED/REFCLK	29
26	1.0	RESERVED/REFCLK	27
24	1.0	RESERVED/REFCLK	25
22	1.0	RESERVED/REFCLK	23
20	1.0	RESERVED/REFCLK	21
18	1.0	RESERVED/REFCLK	19
16	1.0	RESERVED/REFCLK	17
14	1.0	RESERVED/REFCLK	15
12	1.0	RESERVED/REFCLK	13
10	1.0	RESERVED/REFCLK	11
8	1.0	RESERVED/REFCLK	9
6	1.0	RESERVED/REFCLK	7
4	1.0	RESERVED/REFCLK	5
2	1.0	RESERVED/REFCLK	3
1	1.0	RESERVED/REFCLK	2

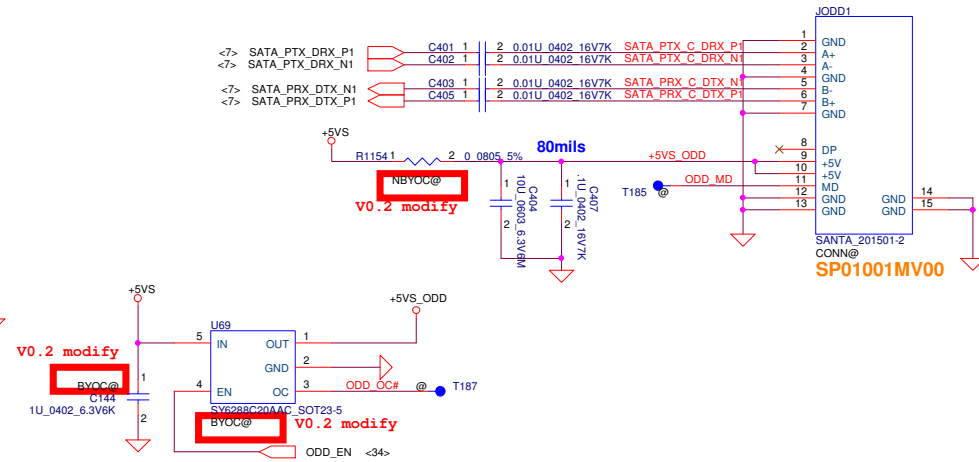
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				Date: Wednesday, March 04, 2015
				Sheet 30 of 55



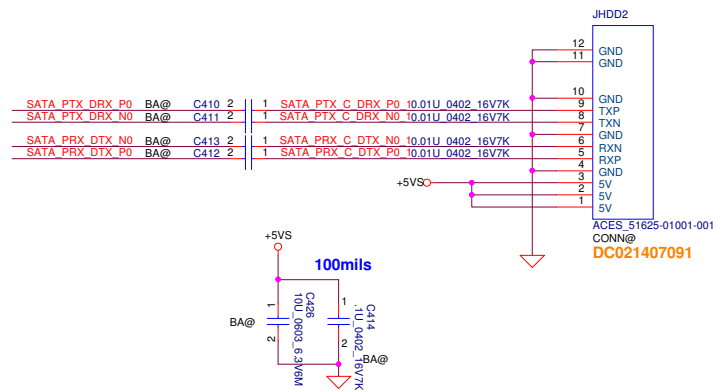
### SATA HDD1 Conn.



### SATA ODD Conn.



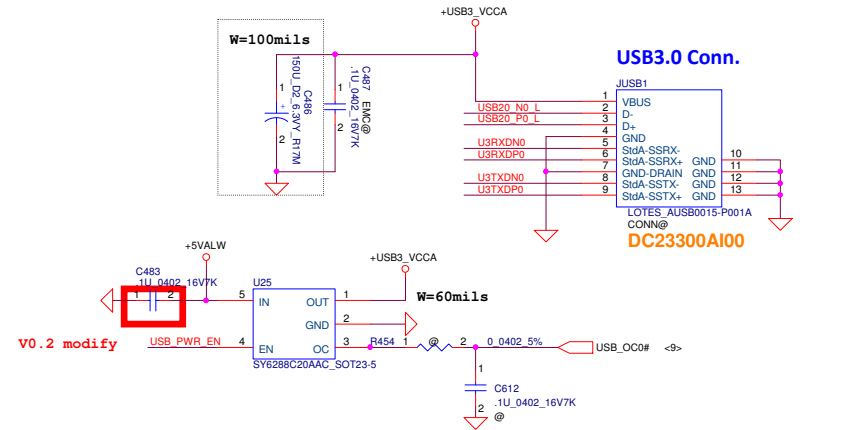
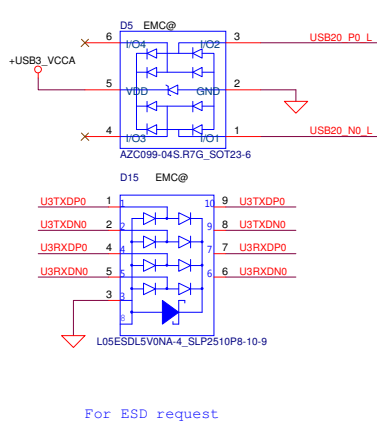
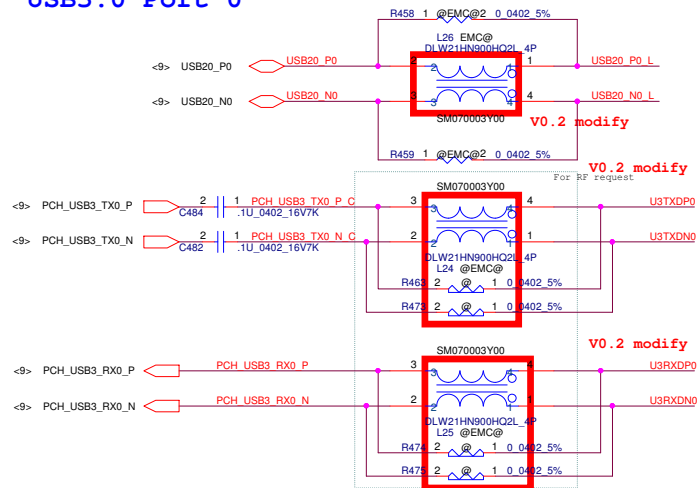
### SATA HDD Conn.



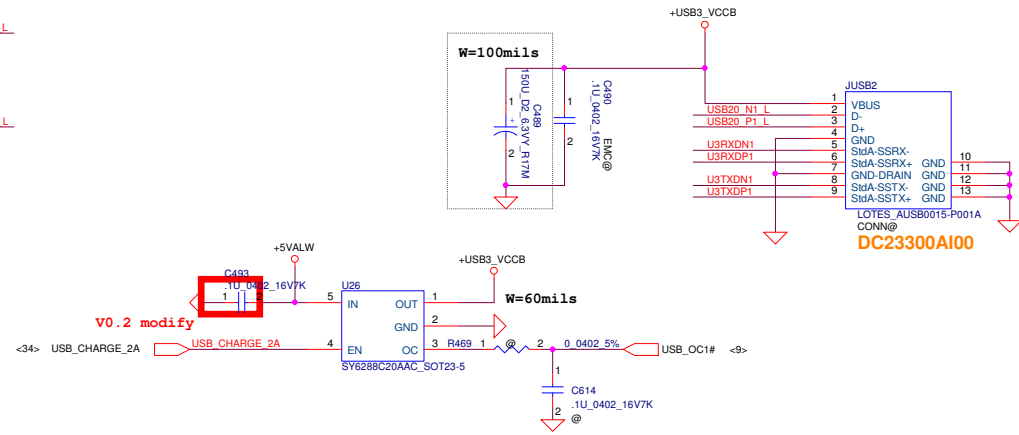
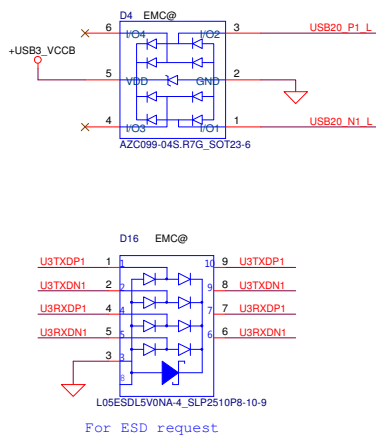
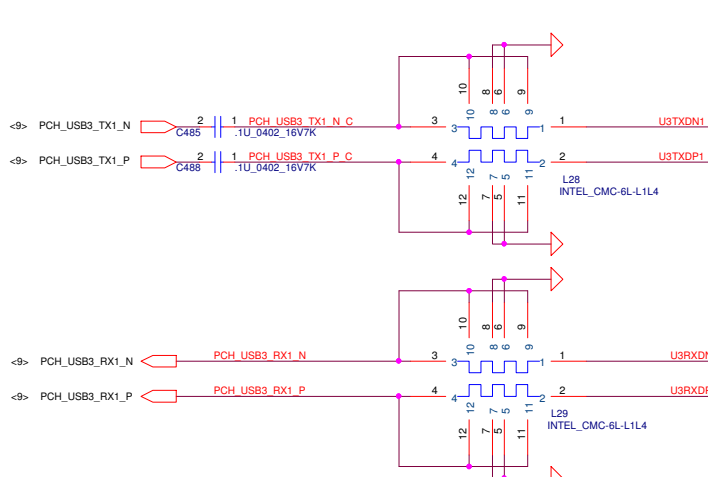
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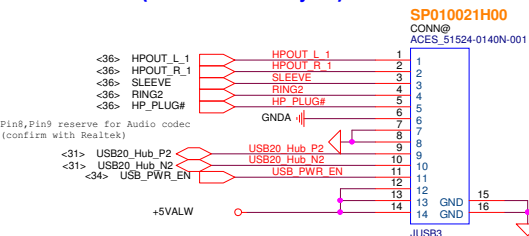
## USB3.0 Port 0



## USB3.0 Port 1

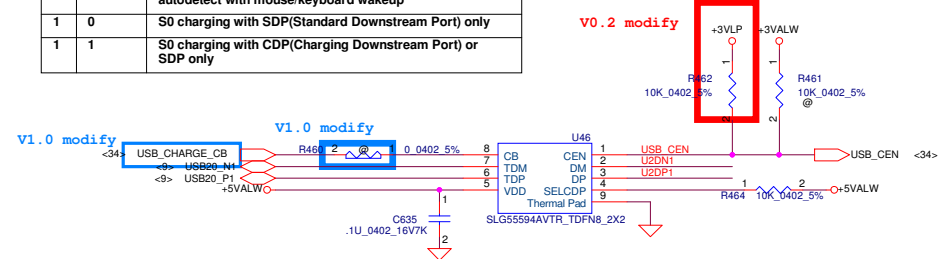


## USB/B Conn. (USB2 x1 + audio jack)

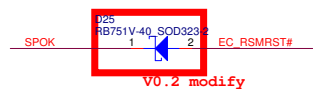


## USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autotdetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only



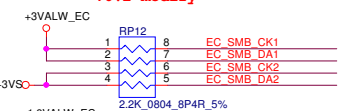
For abnormal shutdown



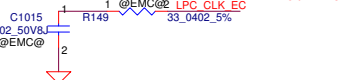
V0.2 modify



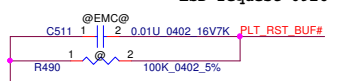
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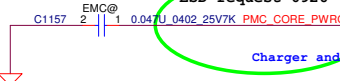
V0.2 modify



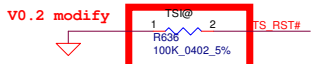
ESD request 0926



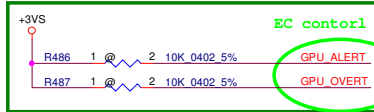
ESD request 0926



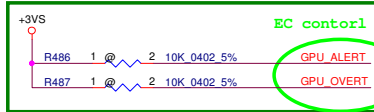
Charger and BATT



V0.2 modify



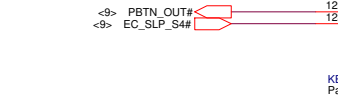
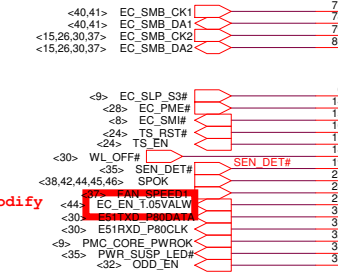
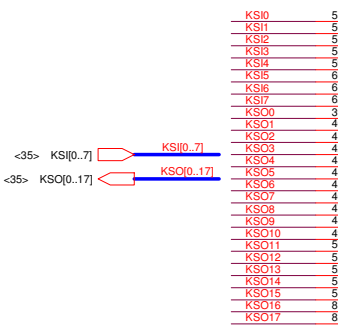
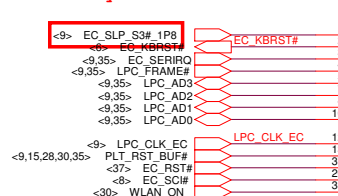
V0.2 modify



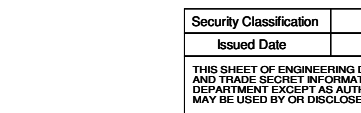
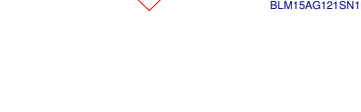
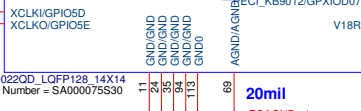
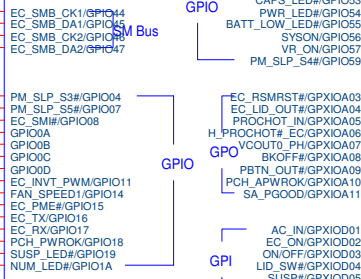
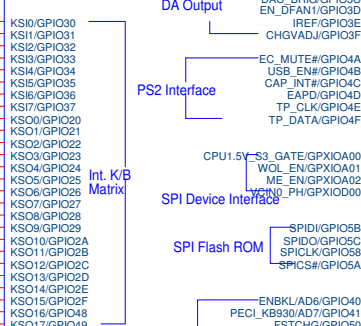
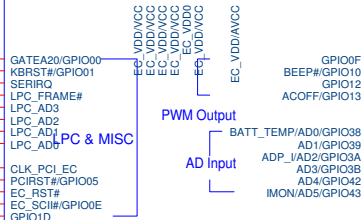
Board ID  
Analog Board ID definition,  
Please see page 3.

Phase	Revision	BID0
EVT	0.1	01
DVT	0.2	02
PVT	1.0	03

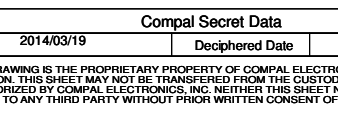
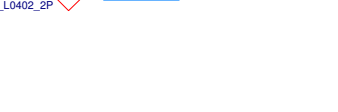
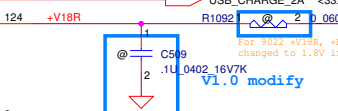
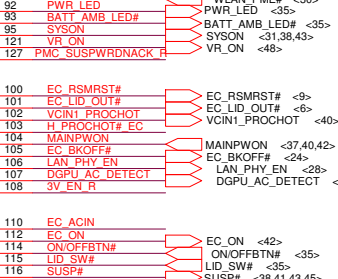
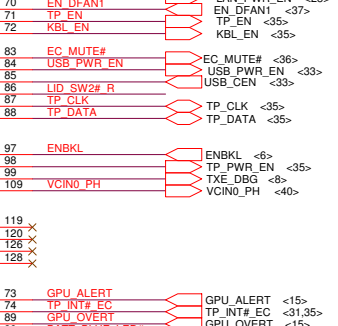
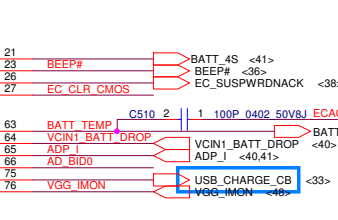
V0.2 modify



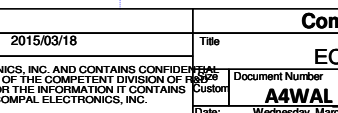
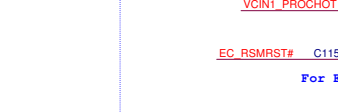
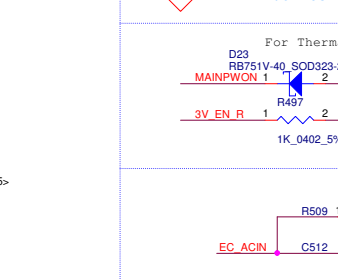
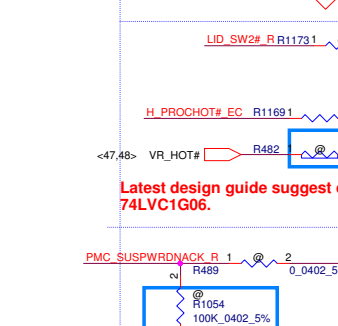
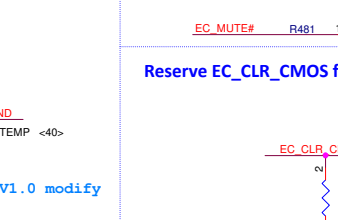
V0.2 modify



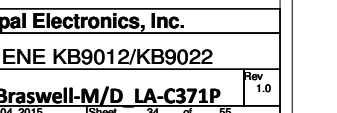
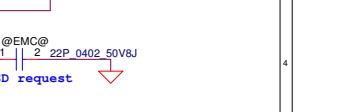
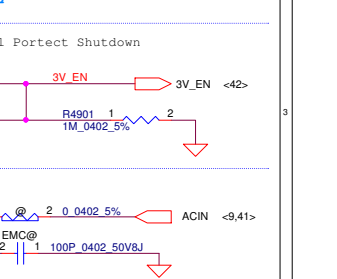
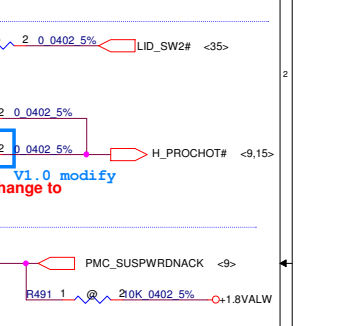
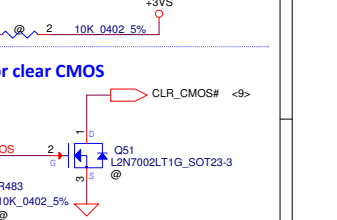
V0.2 modify



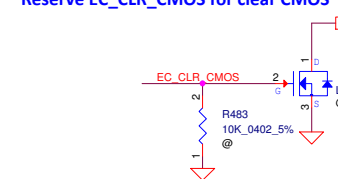
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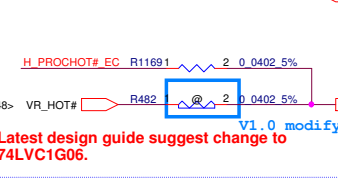
V0.2 modify



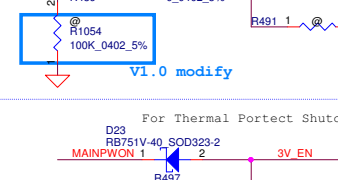
Reserve EC\_CLR\_CMOS for clear CMOS



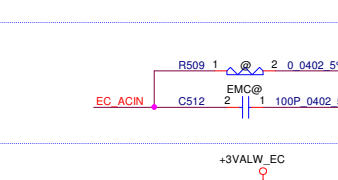
V0.2 modify



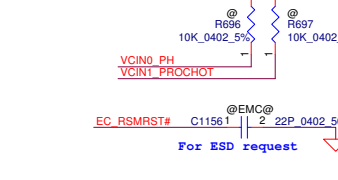
V0.2 modify



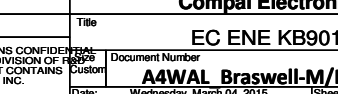
V0.2 modify



V0.2 modify

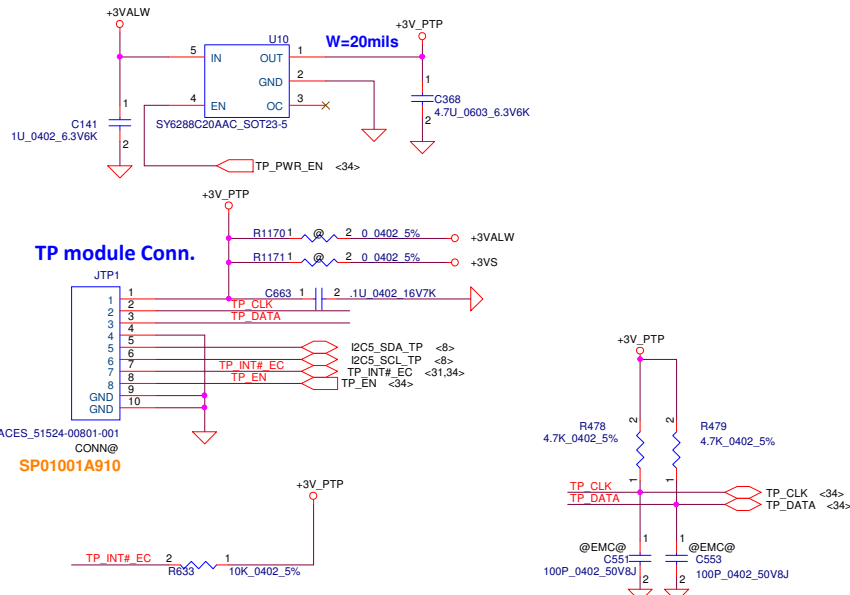
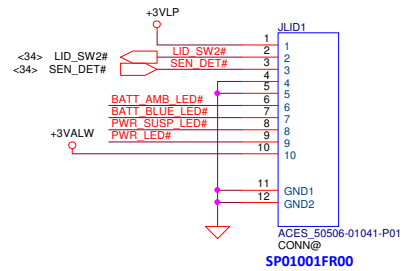


V0.2 modify

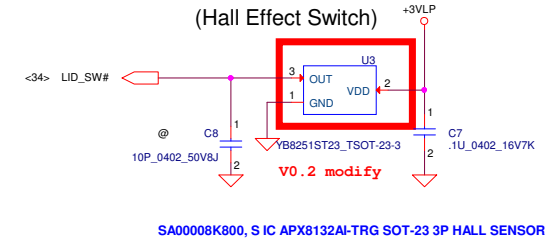


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## Lid Switch 2 (reserve for 15")

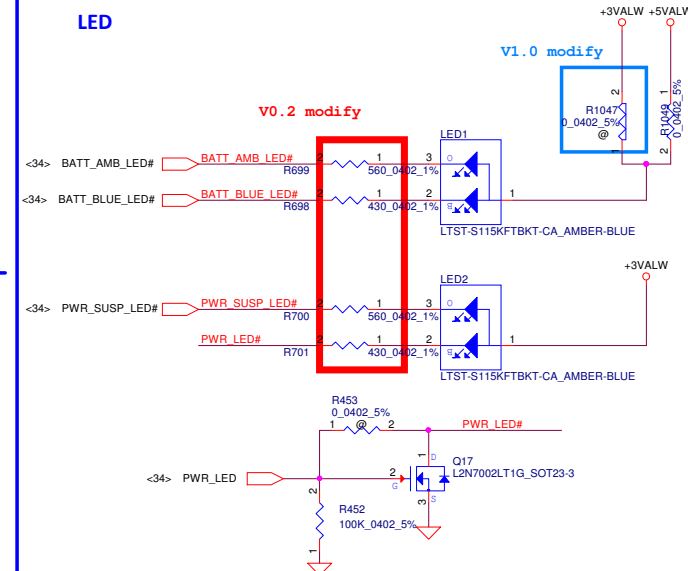


## Lid Switch (Hall Effect Switch)

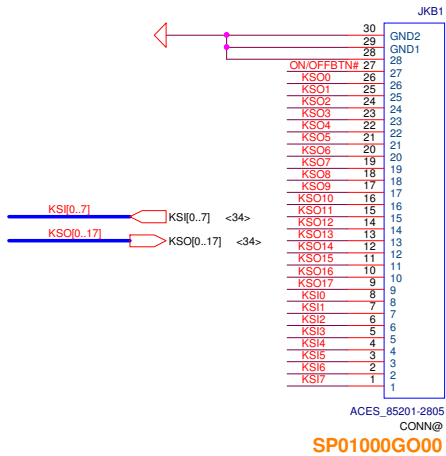


SA00008K800, S IC APX8132AI-TRG SOT-23 3P HALL SENSOR

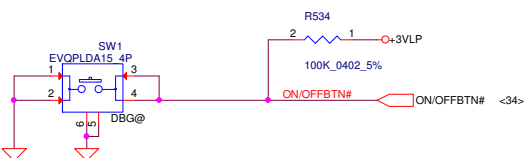
## LED



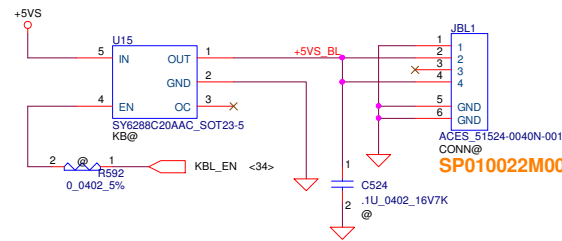
## KB Conn.



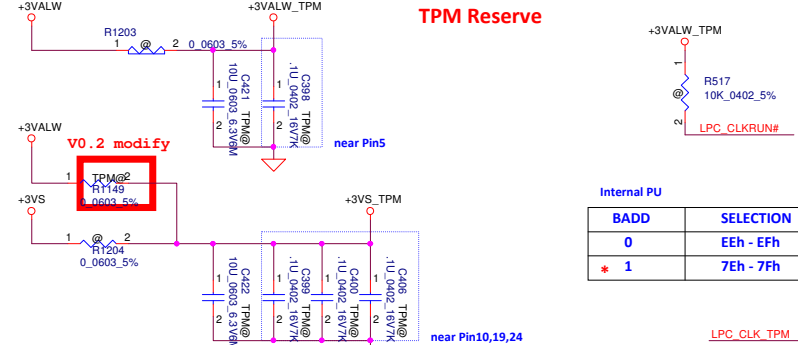
## ON/OFF BTN Test only



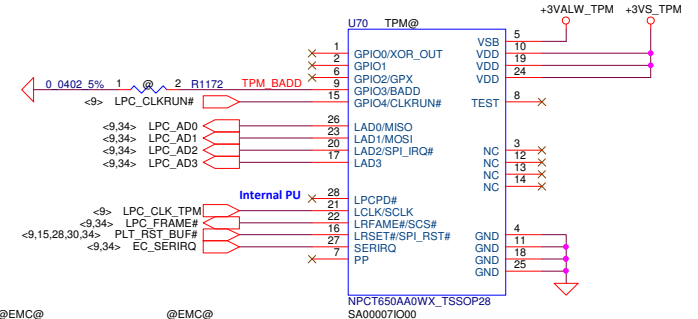
## KB BackLight Conn. Reserve



## TPM Reserve

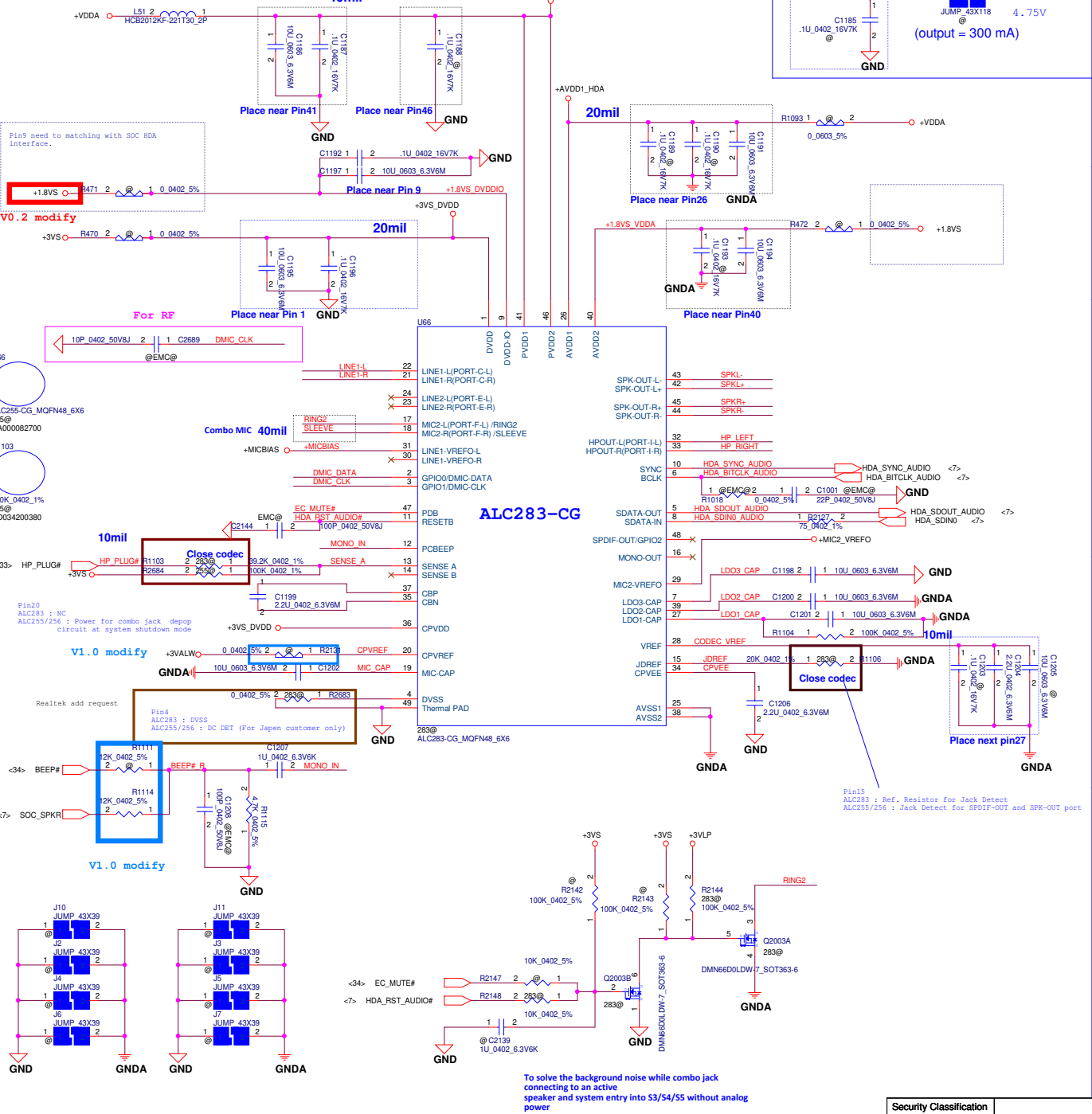


BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh



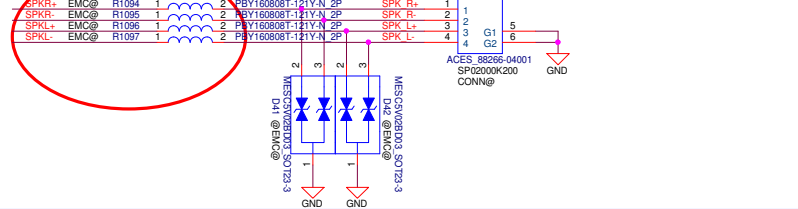
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		SA00007J000	1.0

## M01000EJ00 3000ma 220ohm@100mhz DCR 0.04

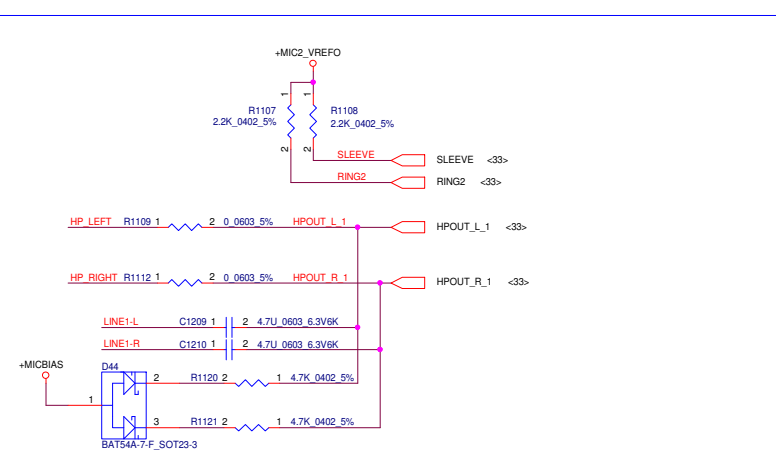
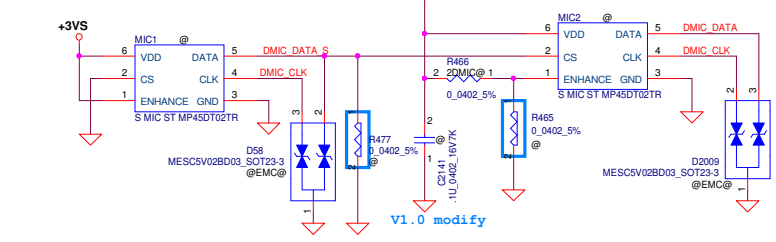


40ml

JSPK1

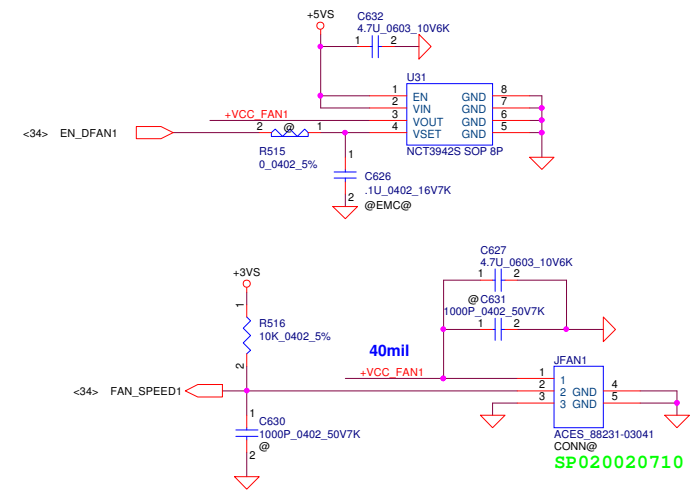


4373

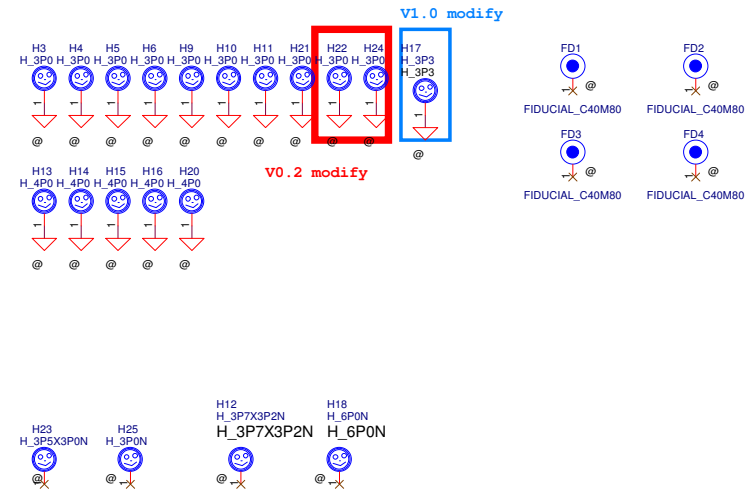


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						HD Audio Codec ALC283/255 colay			
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						Custom	A4WAL Braswell-M/D LA-C371P		1.0
						Date:	Wednesday, March 04, 2015	Sheet	36 of 55

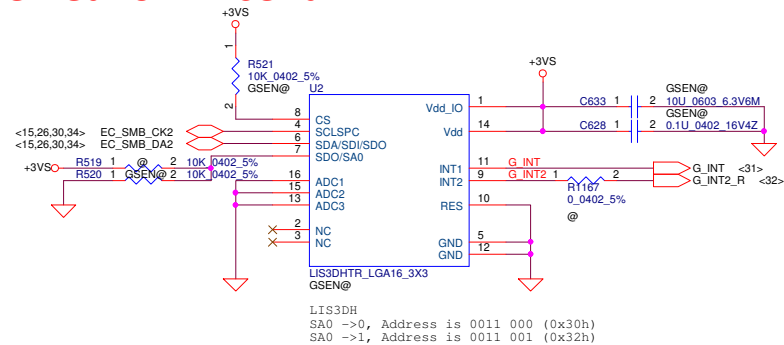
FAN1 Conn



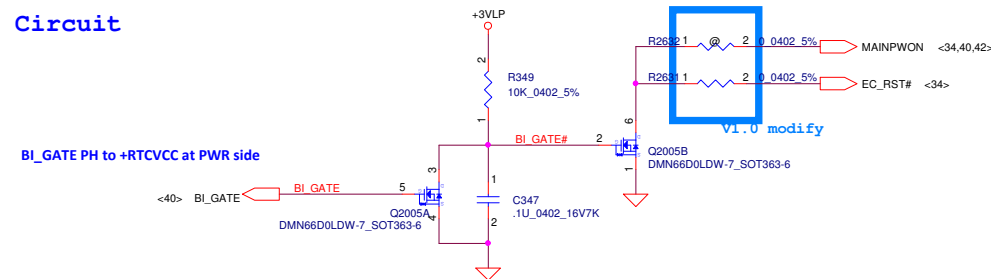
Screw Hole



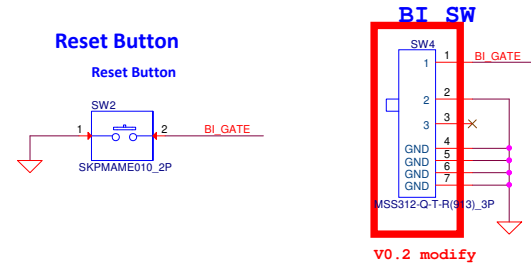
G-Sensor reserved for BA serial



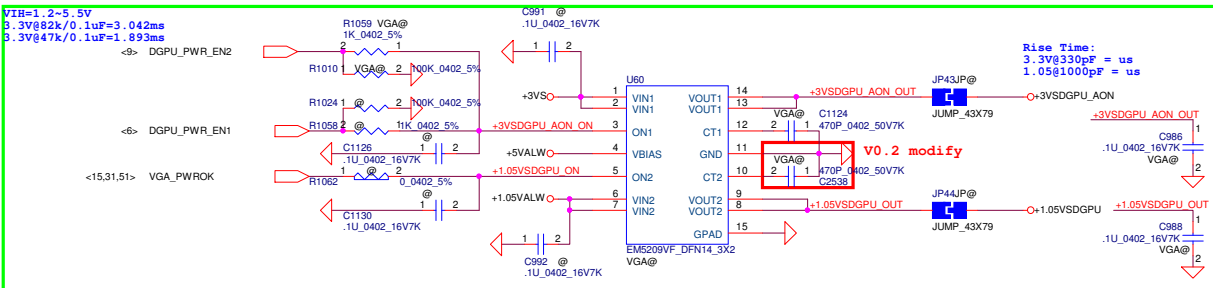
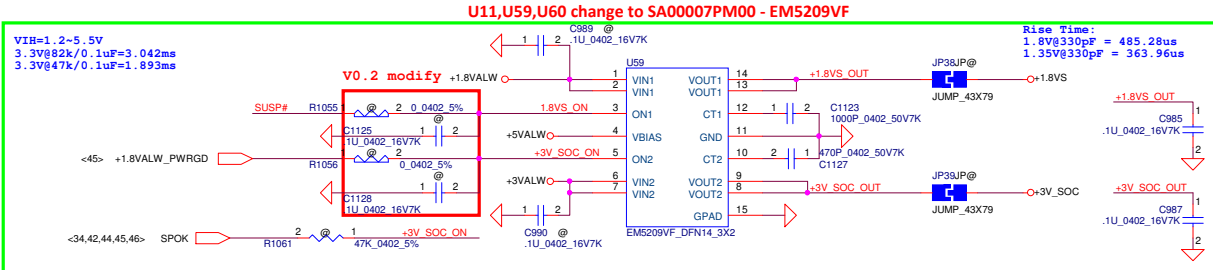
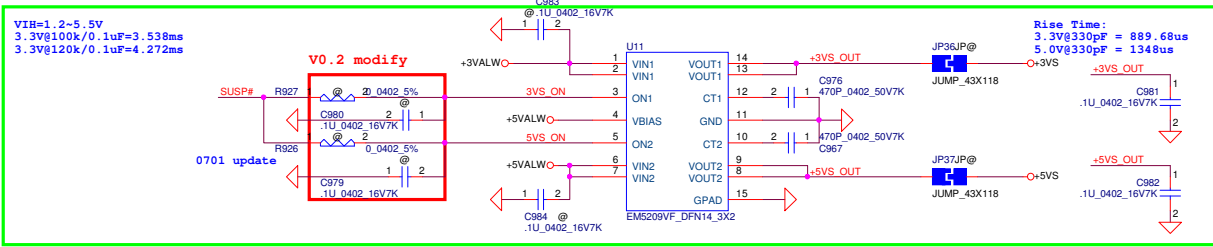
Reset Circuit



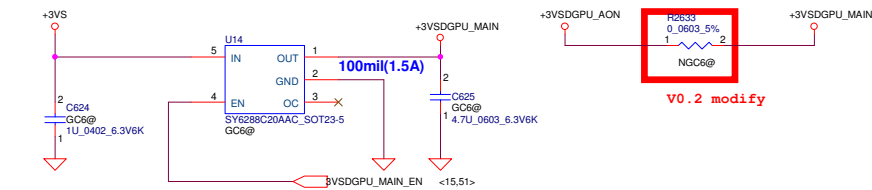
Debug SW



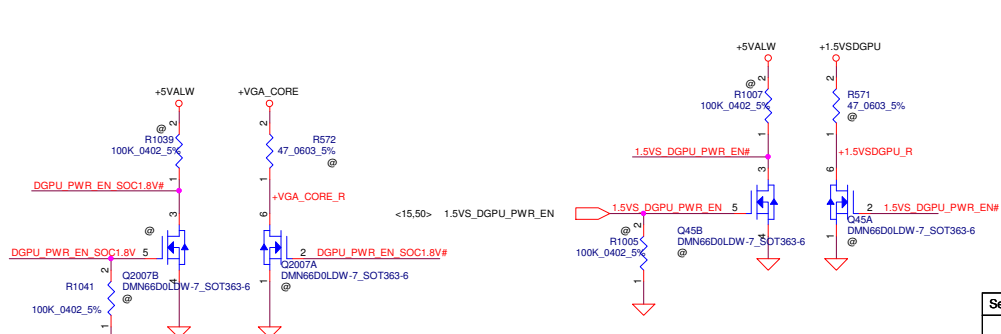
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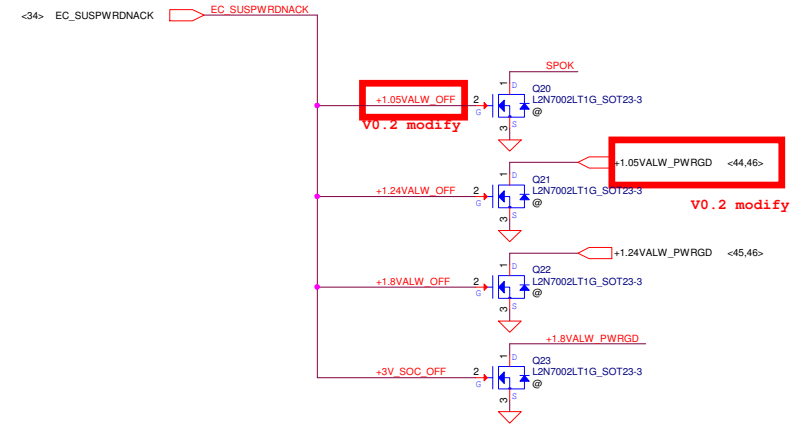
### +3VS to +3VSDGPU\_MAIN for GC6-2.0



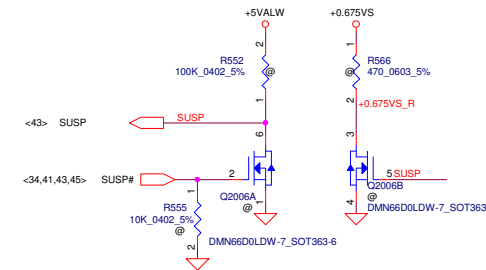
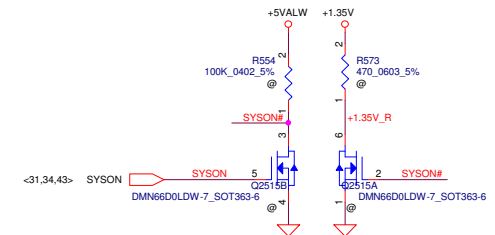
### 3VSDGPU\_MAIN\_EN From GPU



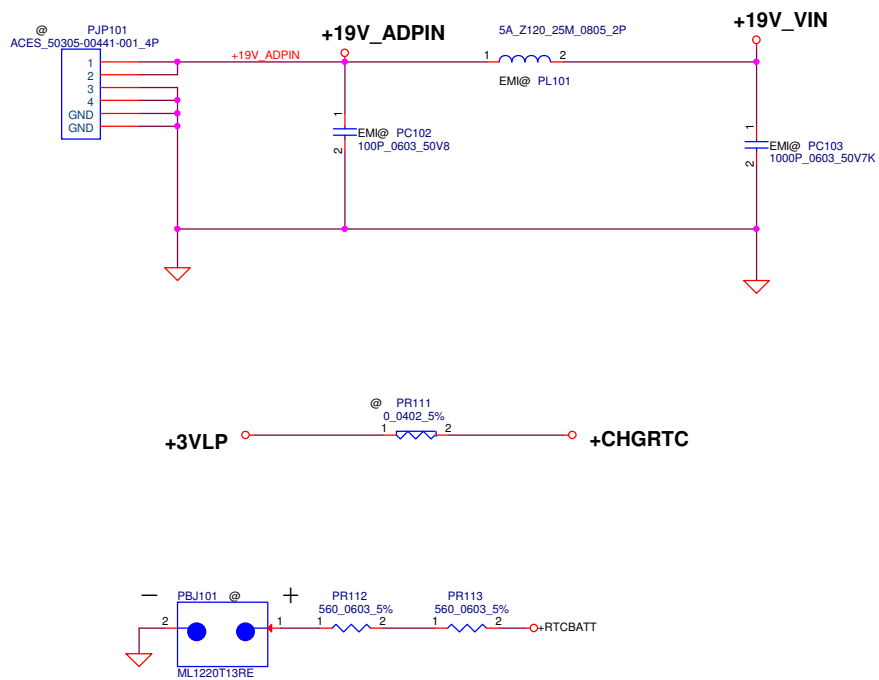
### Power-off sequencing schematic



Q2509,Q2510,Q2511  
Change to SB000001200  
Vgs = 0.49V~1V

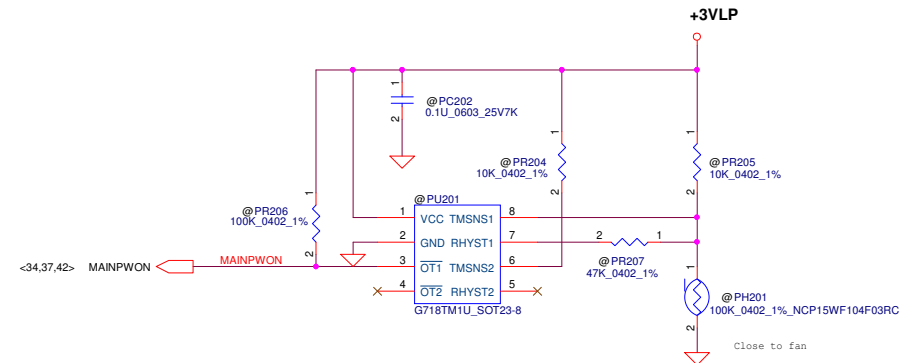
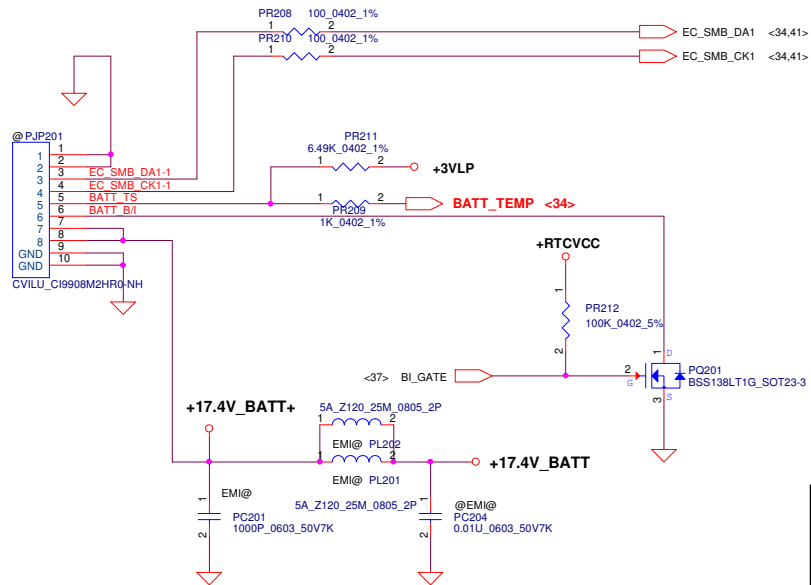


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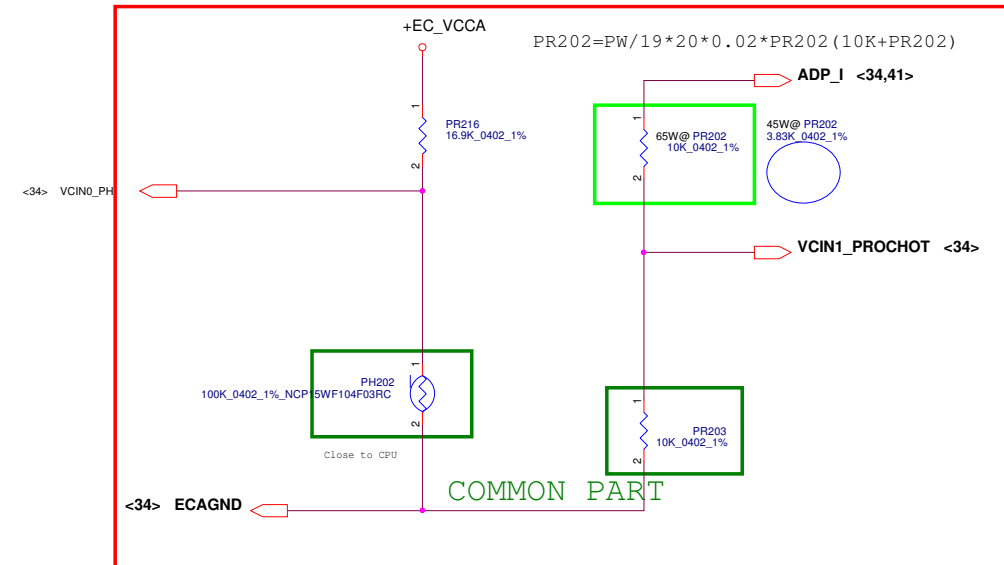
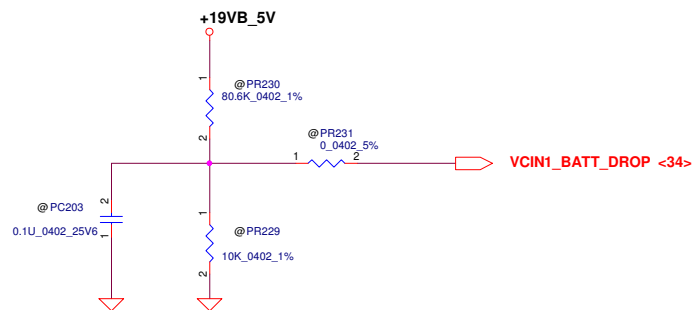




	For KB9022 OTP
92°C	1.0V
56°C	2.0V
PR216	16.9K ohm

Need confirm the setting

For KB9022 sense 20mΩ	Active	Recovery	PR202
65W	69.55W, 0.73V	55.9W, 0.59V	10KΩ
45W	48.15W, 0.73V	38.7W, 0.59V	3.83KΩ



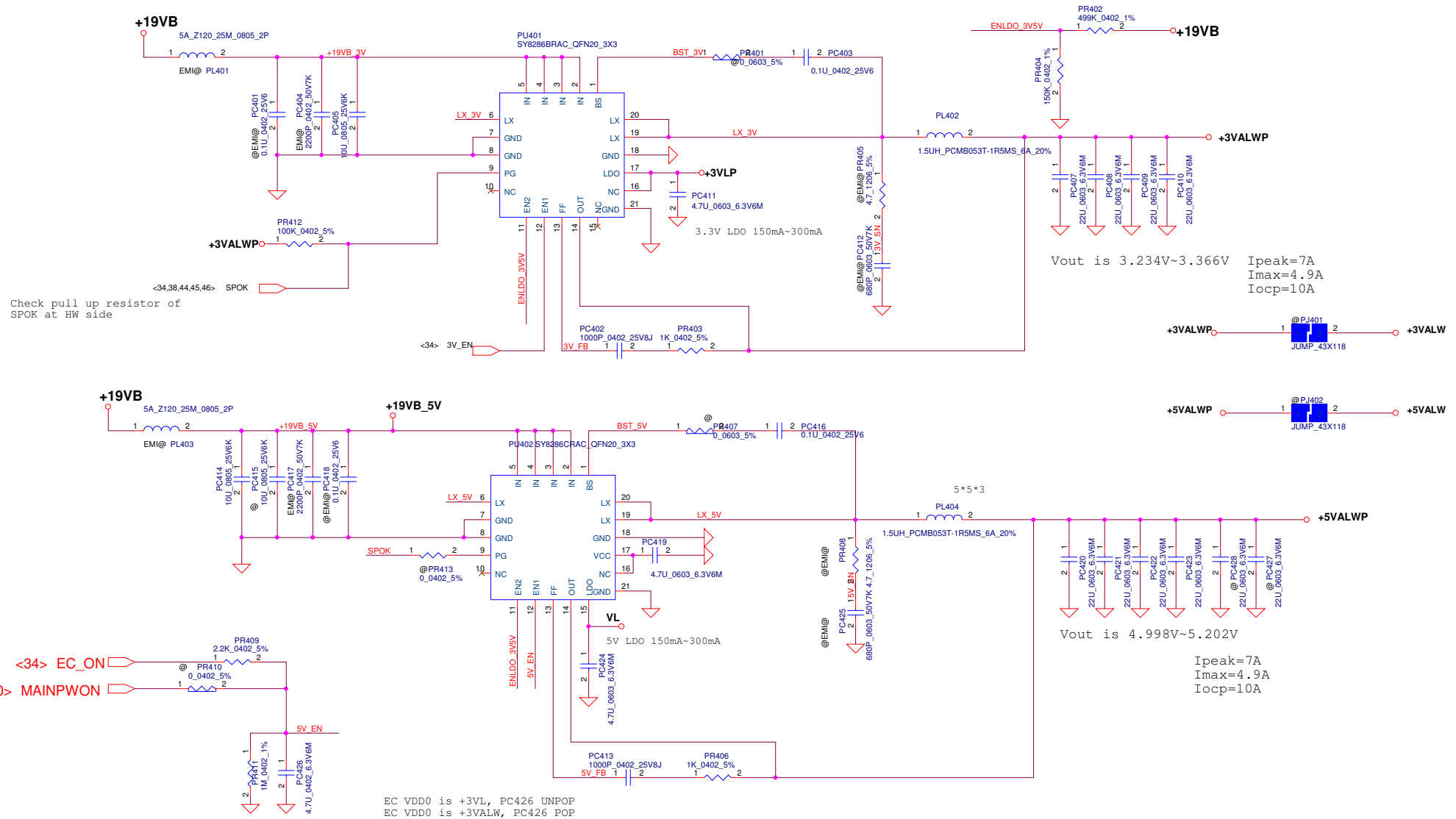
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## Module model information

SY8208B\_V2.mdd

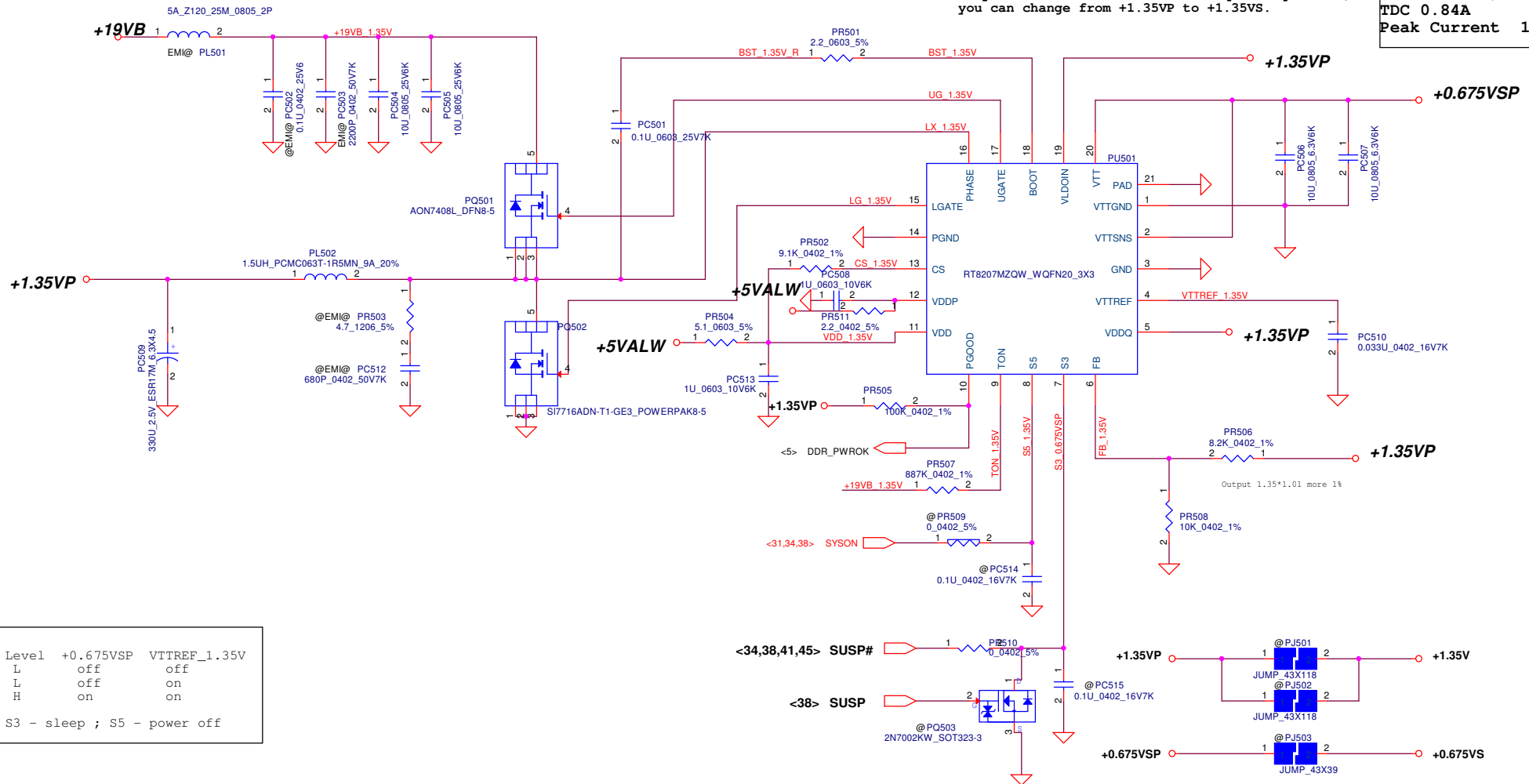
SY8208C\_V2.mdd



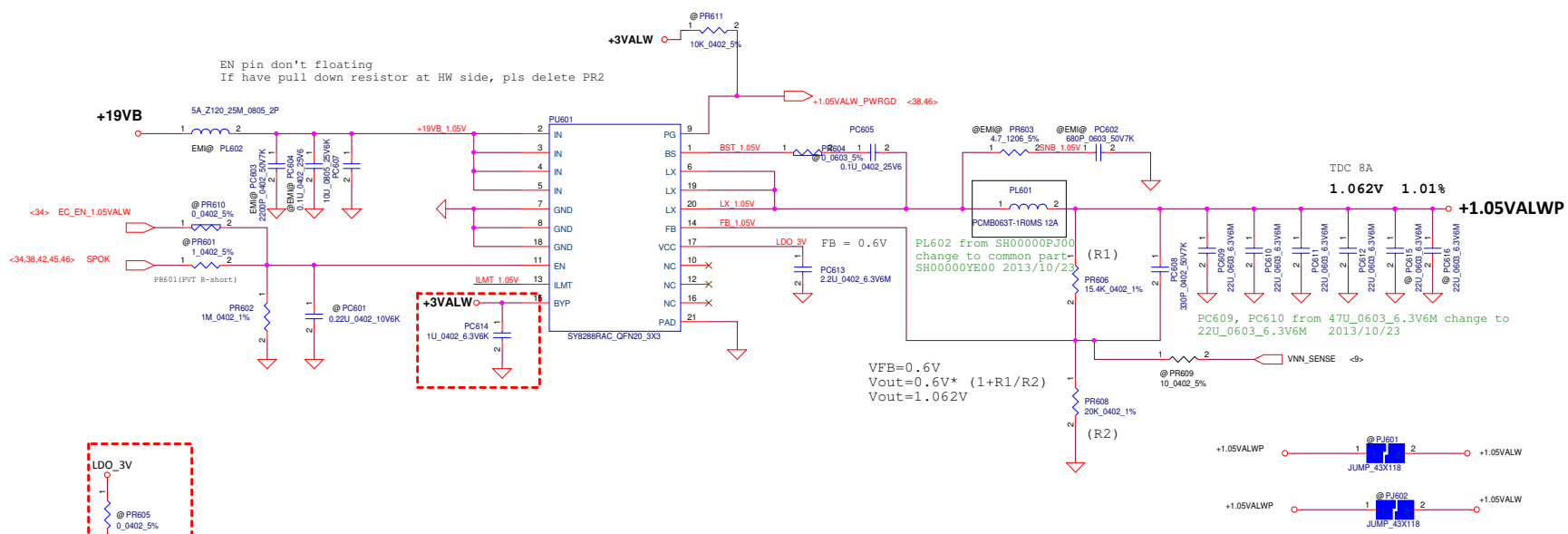
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								3VALW/5VALW	
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Pin19 need pull separate from +1.35VP.  
If you have +1.35V and +0.675V sequence question,  
you can change from +1.35VP to +1.35VS.

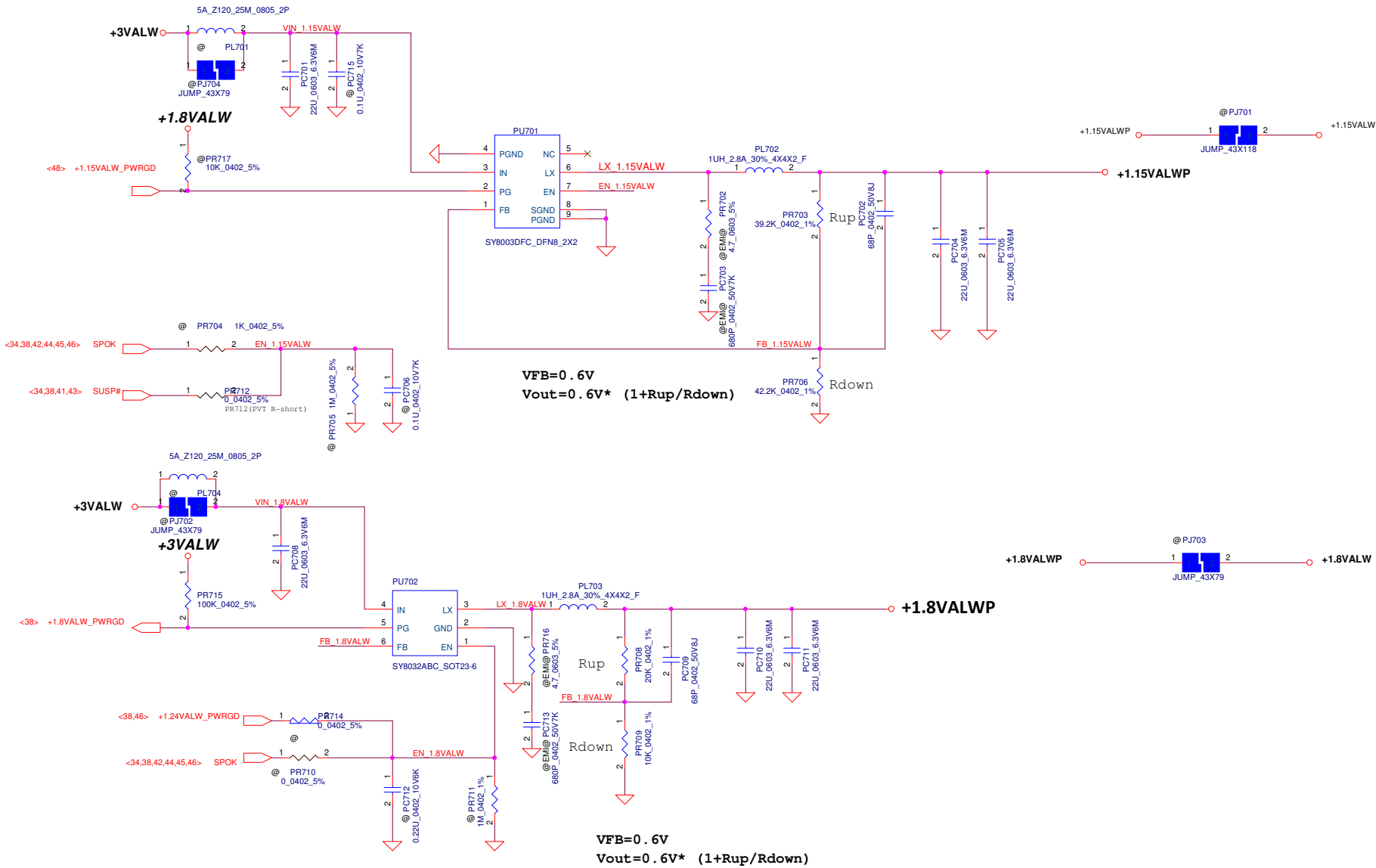
0.675VOLT +/- 5%  
TDC 0.84A  
Peak Current 1.2A



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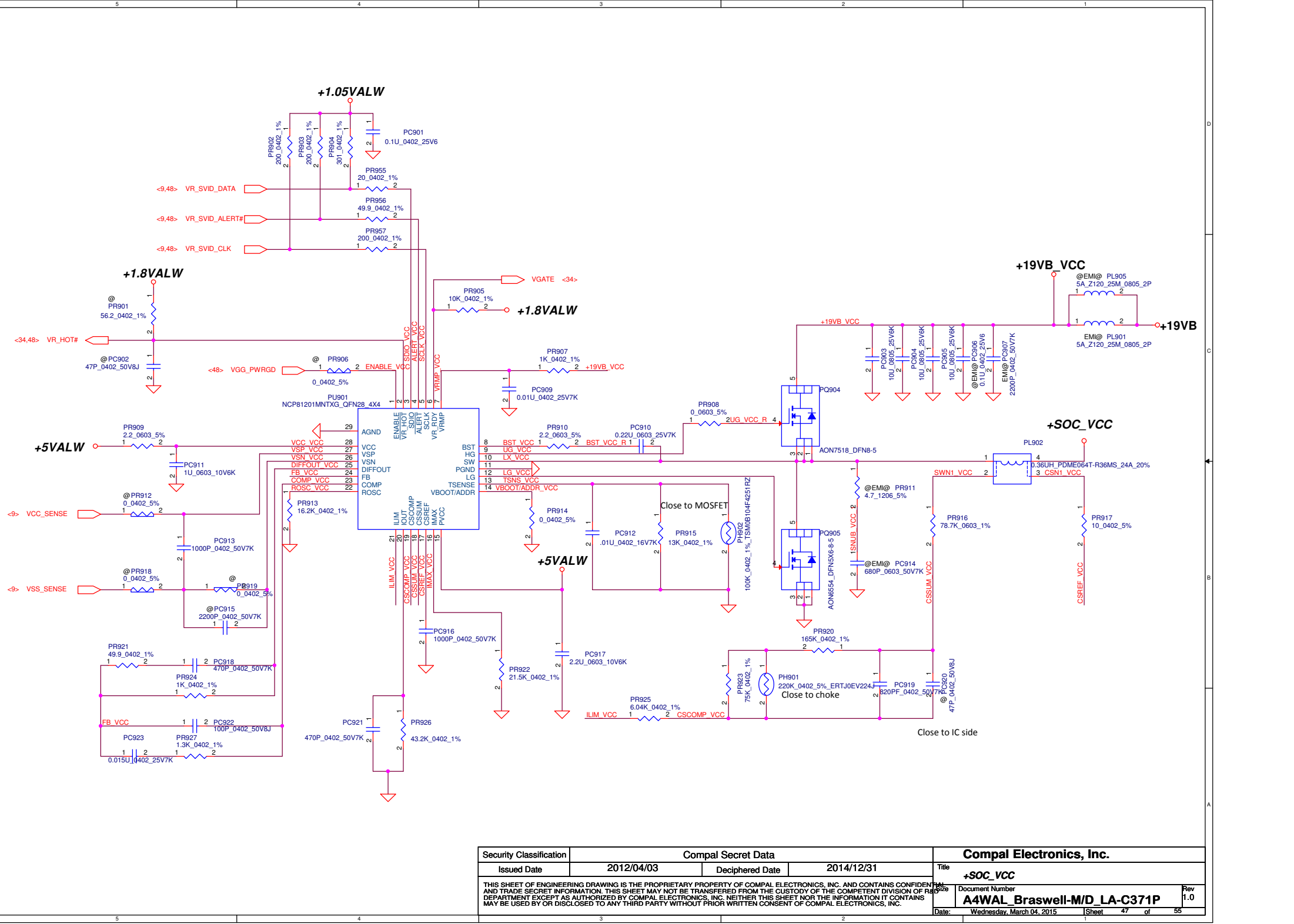
Module model information  
SY8208D\_V1.mdd



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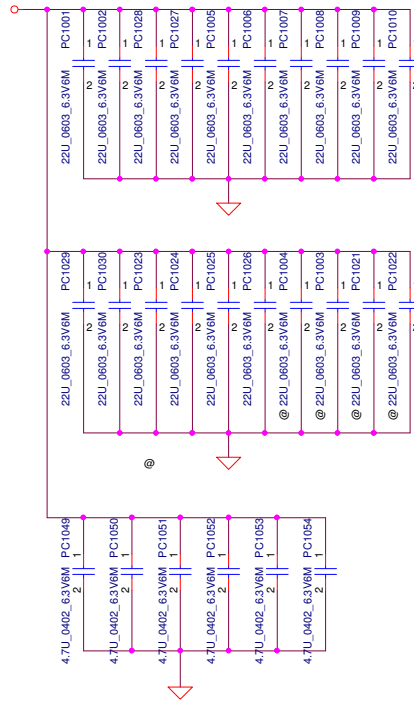


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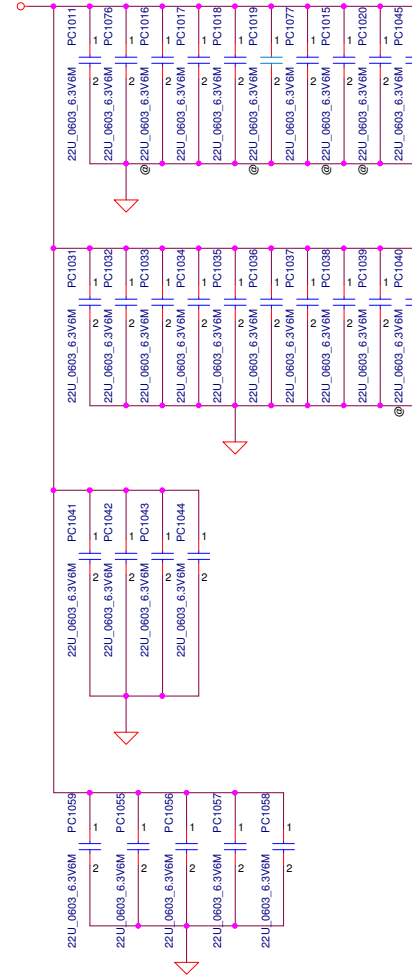
4.7U\_0402 \*5 +22U\_0603 \* 16 + 4 reserved

+SOC\_VCC



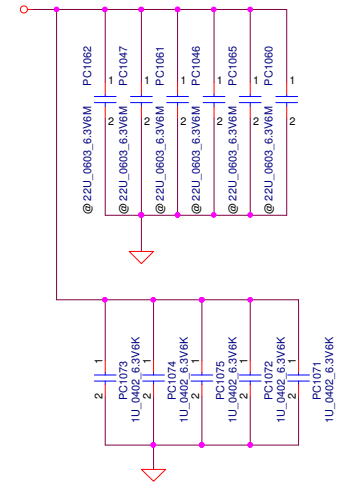
22U\_0603 \* 24 + 5 reserved

+SOC\_VGG



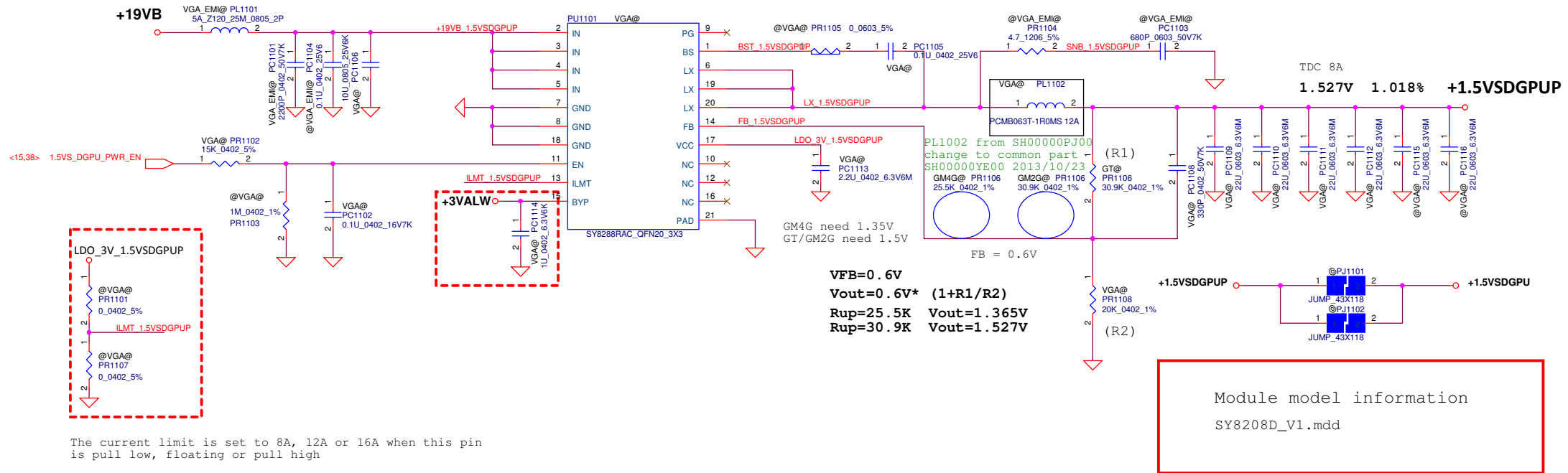
1U\_0402 \* 5+ 22U\_0603\*6 reserved

+1.05VALW



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EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2



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								1.5VSDGPUP	
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EN High Threshold = 1.6V

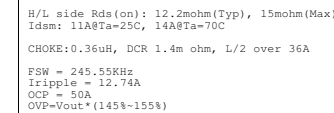
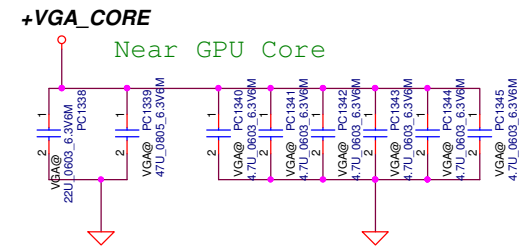
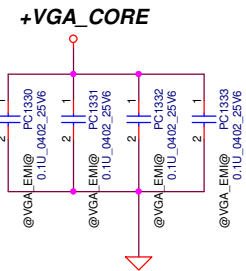
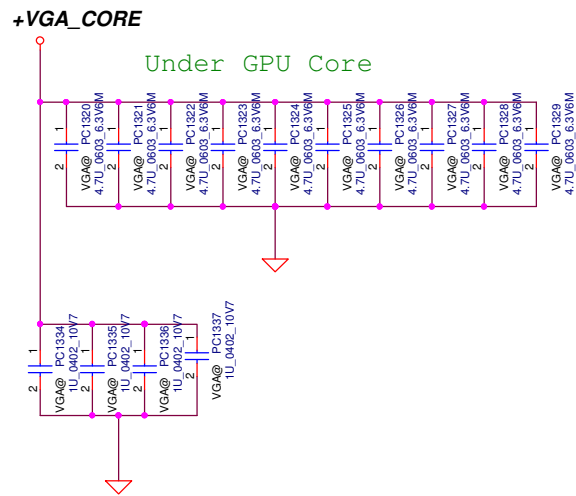


Table 1: PWM-VID options and component values				
PWM-VID Spec		Config B	Config C	Config D
Vmin		0.6V	0.65V	0.9V
Vmax		1.2V	1.15V	1.15V
Vboot		0.9V	0.9V	1.028V
Voltage step		6.25mV	25mV	12.5mV
N of Voltage level		96	20	20
Rrefadj	PR	20K	39K	27K
Rref1	PR	20K	30K	7.5K
Rboot	PR	2K	3K	0
Rref2=PR129 +PR1212	PR	18K	24K	6.2K
	PR	0	3K	1.74K
C	PC	2.7nf	1.8nf	5.6nf

Remove GPU OTP circuit for HW request

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## Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Design update	N16-GM & N16-GT circuit need to use Config B	P.51		SE075562K80 change SE074272K00 PC1210 SD034270280 change SD034200280 PR1209 SD034750180 change SD034200280 PR1208 SD034000080 change SD034200180 PR1211 SD00000GM80 change SD000000580 PR1210 SD034174180 change SD028000080 PR1224 SD034113280 change SD034130280 PR1214	11/20	DVT
2	Design update	3.3V/5V Circuit modify for IC update	P.42		ADD SE00000M000 PC427 PC428 & PU401,PU402	11/28	DVT
3	Design update		P.41		ADD PL301, Remove PJ301	12/04	DVT
4	Design update	1.05V Circuit modify for IC change	P.44			12/04	DVT
5	Design update	VRAM Circuit modify for IC change	P.50			12/04	DVT
6	Design update	1.24V IC Change	P.46		PU801 SA000034S00 change to SA00001HW80	12/04	DVT
7	Design update	SOC_VCC output MLCC adjust	P.49		PC1023 BOM structure change to @	12/15	DVT
8	Design update	Prefer for EC_EN_1.05VALW (turn on SOC suspend)	P.44		ADD EC_EN_1.05VALW Link to circuit	12/15	DVT
9	Design update	ADD PR610 for EC controll	P.44		ADD PR610	12/15	DVT
10	Design update	8207P have spike on S5, so change use ic return to 8207M	P.43		remove PC509.PC511.PC516~PC519, ADDPC509 change RT8207P to RT8207M change PR507 to 887K ohm for frequency	12/16	DVT
11	Design update	common part change			all bead change to SM01000P200	12/16	DVT
12	Design update	1.24V Enable pin need bigger voltage	P.46		PR809 change to R-short PC804 change to "@" PR803 change to 1M and "@"	12/25	DVT
13	Design update	Combine +1.05VALW and +SOC_VNN to +1.05VALW	P.44 & P.49		All SOC_VNN change to 1.05VALW	12/26	DVT
14	Design update	HW sequency change Let efficiency better	P.44 P.46		1.05VALW PG enable 1.24V no pull high PU801 pin6 connect 3VALW	12/26	DVT
15	Design update	HW sequency change	P.45		+1.15VALW EN change to SUP#,	12/26	DVT
16	Design update	PJP201 PCB pad is too short	P.40		Part number change to SP020017H00	12/27	DVT
17	Design update	Let spok signal has rail to discharge	P.44		PR602 Delete"@"	12/27	DVT
18	Design update	Reduce DIS use 0hm pcs	P.51		PR1224,PR1204,PR1207,PR1201,PR1217,PR1219 change to R-short	12/27	DVT
19	Design update	Reduce UMA use 0hm pcs,PVT back to R-short			PR601,PR712,PR329 change to 1ohm PR933,PR906 change to R-short	12/27	DVT
20	Design update	Follow HW command	P.50		PR1102 change to 10K	12/29	DVT
21	Design update	Follow FAE command			PC403,PC416,PC605,PC1105 change to 0.1U_0603_25V7K	12/31	DVT
22	Design update	Design for HW sequency need	P.41		Add PR321 (BOM Structure :@) link to +3VLP	1/7	PVT
23	Design update	Design for sourcer need	P.43		Change PQ502 to AON7702	1/8	DVT
24	Design update	Follow HW command			PR610 instead PR601 PR509 PR510 change to 1 ohm PC515 change to @ PR1102 change to 15k	1/8	DVT
25	Design update	Follow HW command-1.24V	P.46		POP PR803	1/12	DVT
26	Design update	Change for 1.35V Power budget current limit	P.43		Change PR502 to 9.1K	2/3	PVT
27	Design update	Change all 1 ohm to 0 ohm for PVT			Change PR329.PR509.PR510.PR610.PR712 to 0 ohm	2/6	PVT
28	Design update	Follow HW command	P.47 P.44		PR901 unplug & 1.05V PG pull high resistor"@" 3V & 5V IC Pin 16 connect Pin17	2/10	PVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Design update	Follow HW command	P.42		1.PR5090,PR610改為R short 2.1.15VALW的 PG多一跟pin ,net name 為+1.15VALW_PWRGD, 然後預留PU 10K ohm 1.8VALW. 3.將+1.15VALW_PWRGD串接一顆0ohm 然後@,接到VGG的ENABLE,同時將PR933的R short改為上件	2/12	PVT
2	Design update						
3	Design update						
4	Design update						
5	Design update						
6	Design update						
7	Design update						
8	Design update						
9	Design update						
10	Design update						
11	Design update						
12	Design update						
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18	Design update						
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21	Design update						
22	Design update						
23	Design update						
24	Design update						
25	Design update						
26	Design update						
27	Design update						
28	Design update						PVT

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SOC

0.2 modify

VGA

VGA not ready

Plug in

S5->S0

S0->S3

S3->S0

S0->S5

DC mode

ACIN

+3VLP

EC\_ON

+5VALW

3V\_EN

+3VALW

SPOK

EC\_EN\_1.05VALW

+1.05VALW (VNN)

+1.24VALW

+1.8VALW

+3V\_SOC

ON/OFF

EC\_RSMRST#

PBTN\_OUT#

EC\_SLP\_S4#

EC\_SLP\_S3#\_1P8

SYSON

+1.35V

DDR\_PWROK

VR\_ON

+SOC\_VGG

+SOC\_VCC0/1

VGATE

SUSP#

+1.15VALW

+1.8VS

+3VS

+5VS

+0.675VS

KBRST#

PMC\_CORE\_PWROK

DDR\_CORE\_PWROK

PMC\_PLTRST#

DGPU\_PWR\_EN

+3VSDGPU

VGA\_CORE

VGA\_PWROK

+1.05VSDGPU

+1.5VSDGPU

PLTRST\_VGA#

ACIN

+3VLP

EC\_ON

+5VALW

3V\_EN

+3VALW

SPOK

EC\_EN\_1.05VALW

+1.05VALW (VNN)

+1.24VALW

+1.8VALW

+3V\_SOC

ON/OFF

EC\_RSMRST#

PBTN\_OUT#

EC\_SLP\_S4#

EC\_SLP\_S3#

SYSON

+1.35V

DDR\_PWROK

VR\_ON

+SOC\_VGG

+SOC\_VCC0/2

VGATE

SUSP#

+1.15VALW

+1.8VS

+3VS

+5VS

+0.675VS

KBRST#

PMC\_CORE\_PWROK

DDR\_CORE\_PWROK

PMC\_PLTRST#

DGPU\_PWR\_EN

+3VSDGPU

VGA\_CORE

VGA\_PWROK

+1.05VSDGPU

+1.5VSDGPU

PLTRST\_VGA#

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				Date:	Wednesday, March 04, 2015	Sheet 55 of 55